MOTOROLA

PENT/ATCA–717

Reference Guide

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Using This Guide

This Reference Guide is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), AdvancedTCA®, and telecommunications.

Conventions

Notation	Description
57	All numbers are decimal numbers except when used with the notations described below.
00000000_{16} or 0x00000000	Typical notation for hexadecimal numbers (digits 0 through F), e.g. used for addresses and offsets
0000_2 or 0b0000	Same for binary numbers (digits are 0 and 1)
x	Generic use of a letter
n	Generic use of numbers
0.75	Decimal number
Bold	Used to emphasize a word
`Courier`	Used for on-screen output
`Courier+Bold`	Used to characterize user input
Italics	For references, table, and figure descriptions
<text>	Notation for variables and keys
[text]	Notation for buttons and optional parameters
...	Repeated item (example: A1, A2, A3, ..., A12)
Note:	No danger encountered. Pay attention to important information
Caution	Possibly dangerous situation: slight injuries to people or damage to objects possible

Notation	Description
	Dangerous situation: injuries to people or severe damage to objects possible

Abbreviations

Abbreviation	Description
A	
AC	Alternating Current
ANSI	American National Standards Institute
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
ATA	Advanced Technology Attachment
ATCA	Advanced Telecommunications Computing Architecture
B	
BIOS	Basic Input/Output System
BMC	Base Board Management Controller
C	
CMC	Common Mezzanine Card
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
D	
DDR	Double Data Rate
DMA	Direct Memory Access
DPLL	Digital Phase Locked Loop
DRAM	Dynamic Random Access Memory
E	
ECC	Error-Correction Code
EMC	Electromagnetic Compatibility
EN	European Norm
ESCD	Extended System Configuration Data
ESD	Electrostatic Sensitive Device
F	
FAE	Field Application Engineers

Abbreviation	Description
FCC	Federal Communications Commission
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
FRU	Field Replacable Unit
G	
GND	Ground
I	
IDE	Integrated Device Electronics
IEC	International Electric Code
IPMB	Intelligent Platform Management Bus
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
ISA	Industry Standard Architecture
ISO	International Organization for Standardization
L	
LCCB	Line Card Clock Building Block
LED	Light Emitting Diode
LFM	Linear Feet per Minute
LPC	Low Pin Count
M	
MAC	Media Access Control
N	
NEBS	Network Equipment Building System
NVRAM	Nonvolatile Random Access Memory
O	
OEM	Original Equipment Manufacturer
OOS	Out-Of-Service
P	
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PEM	Power Entry Module
PICMG	PCI Industrial Computer Manufacturers Group
PMC	PCI Mezzanine Card
POST	Power-On Self-Test
PROM	Programmable Read-Only Memory

Abbreviation	Description
R	
RAM	Random Access Memory
ROM	Read-Only Memory
RTC	Real Time Clock
RTM	Rear Transition Module
S	
S.M.A.R.T.	Software Maintenance and Reference Tool
SATA	Serial ATA
SCSI	Small Computer System Interface
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SELV	Safety Extra Low Voltages
SMI	Serial Management Interface
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SROM	Serial Read-Only Memory
U	
UL	Underwriters Laboratory Inc.
USB	Universal Serial Bus
V	
VGA	Video Graphics Array
VLAN	Virtual Local Area Network

Revision History

Order No.	Rev.	Date	Description
222282	AA	June 2004	Preliminary Reference Guide
222282	AB	January 2005	Final release version
222282	AC	February 2005	Corrected naming of Ethernet controllers Intel 82546EB/GB and 82540EM
225444	AA	March 2005	Corrected figure showing the switch locations; corrected description of SW4-1 default setting; enhanced description of redundant BIOS feature

Order No.	Rev.	Date	Description
226132	AA	May 2005	Changed logo, copyright, ... from Force Computers to Motorola;generalized safety notes regarding maximum combined power dissipation of installed PMC modules; in power requirements: added exceptions applicable to US and Canada; in standard compliances: removed IEC60068 (officially withdrawn) and UL94V–0/1 (already covered by 60950 and NEBS) standard; added section ″Restoring BIOS Default Settings″; added ″Restore BIOS Default Settings″ procedure; added info on redundant FPGA feature (section Devices Features and Datapaths–>FPGA); in switch setting description and Flashes section: renamed boot flash to default flash and user flash to backup flash; extended description of redundant flash feature; in standard compliances section: added note on NEBS compliance and grounding; adapted figures showing the blade face plate to new Motorola face plate; added note to section ″Updating BIOS″; updated list of IPMI sensors in section: Intelligent Platform Management Controller in section ″Switch Settings″ extended description of ″Clear CMOS RAM″ and ″Serial COM port swapping″ switch ; extended section BIOS–>Serial Console Redirect–>Default Configuration; added section ″About this Manual″

Order No.	Rev.	Date	Description
6806800A15A		April 2006	Created separate manual for blade used in AXP systems; Changed parallel ATA connector pinout; modified description of on–board switches SW4–1, SW4–2 and SW4–4 (default settings were changed); updated description of Ethernet switch configuration (new routing); updated PMC Pn4 pinout description; extended description of face plate LEDs; updated description of P23 backplane connector pinout; added section: BIOS–>Crisis Recovery Mode; updated on–board switch description: crisis recovery switch no more reserved;changed location of two temperature sensors and adapted list of IPMI sensors; removed references to full mesh routing: no longer an available option; in blade installation: removed warning regarding plastic handles (new handles are used now); updated ordering information

Other Sources of Information

For further information refer to the following documents.

Note: Check the Motorola literature catalog for errata sheets that may be applicable to the blade.

Company or Organisation	www.	Document
Motorola	motorola.com/computing	ACC/ARTM-717 Installation Guide
		ACC/CABLE/RJ45/DSUB Installation Information
		ACC/ATCA-715/HDD Installation Guide
		ACC/ATCA-715/HDD-SATA Installation Guide
		ACC/ATCA – CMC – MODULE Installation Guide.
		PENT/ATCA-715/717/7105/7107: Control via IPMI Programmer's Guide Guide
		PENT/ATCA-715/717/7105/7107 BIOS Information Sheet
Intel	intel.com	6300ESB I/O Controller Datasheet
		82540EM Gigabit Ethernet Controller Documentation
		82546EB/GB Gigabit Ethernet Controller Documentation
		82802AC Firmware Hub (FWH) Datasheet
		82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet
		E7501 Memory Controller Datasheet
		IPMI V1.5 Specifications
		Pentium M Processor Technical Documents
Marvell	marvell.com	Prestera DX160 16-Port Gigabit Ethernet Packet Processor Documentation
PCI-SIG	pcisig.com	PCI Local Bus Specification Revision 2.2 PCI-X Addendum to the PCI Local Bus Specification 1.0

Company or Organisation	www.	Document
PICMG	picmg.org	PICMG 3.0 Revision 1.0 Advanced TCA Base Specification PICMG 3.1 Revision 1.0 Specification Ethernet/Fiber Channel for AdvancedTCA Systems
SMSC	smsc.com	LPC47S422 Enhanced Super I/O Controller Datasheets and Application Notes

Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the product.

We intend to provide all necessary information to install and handle the product in this manual. However, as the product is complex and its usage manifold, we do not guarantee that the given information is complete. If you need additional information, ask your Motorola representative.

The product has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Motorola or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

EMC

The blade has been tested in a standard Motorola system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules, EN 55022 Class A respectively. These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial environment.

The blade generates and uses radio frequency energy and, if not installed properly and used in accordance with this guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Installation

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD–safe environment.

Data loss
Removing the blade with the blue LED still blinking causes data loss.
Wait until the blue LED is permanently illuminated, before removing the blade.

Damage of Blade and Additional Devices and Modules
Incorrect installation of additional devices or modules may damage the blade or the additional devices or modules.
Before installing or removing an additional device or module, read the respective documentation

Operation

Blade damage
Blade surface
High humidity and condensation on the blade surface causes short circuits.
Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power.
Do not operate the blade below 0˚C.

Blade Overheating and Blade Damage
Operating the blade without forced air cooling may lead to blade overheating and thus blade damage.
When operating the blade, make sure that forced air cooling is available in the shelf.

When operating the blade in areas of electromagnetic radiation ensure that the blade is bolted on the system and the system is shielded by enclosure.

Injuries or short circuits
Blade or power supply
In case the ORing diodes of the blade fail, the blade may trigger a short circuit between input line A and input line B so that line A remains powered even if it is disconnected from the power supply circuit (and vice versa).
To avoid damage or injuries, always check that there is no more voltage on the line that has been disconnected before continuing your work.

Switch Settings

Blade Malfunction
Switches marked as 'reserved' might carry production–related functions and can cause the blade to malfunction if their setting is changed.
Therefore, do not change settings of switches marked as 'reserved'. The setting of switches which are not marked as 'reserved' has to be checked and changed before blade installation.

Blade Damage
Setting/resetting the switches during operation can cause blade damage.
Therefore, check and change switch settings before you install the blade.

Environment

Always dispose of used blades according to your country's legislation, if possible in an environmentally acceptable way.

PMC Modules

Limited Power on PMC Modules and RTMs
The blade does not provide an extra fuse for PMC modules and RTMs.
PMC modules and RTMs used together with the blade have to be qualified according to the following standards: IEC 60950–1, EN 60950–1, UL 60950–1, CAN/CSA C22–2 No 60950–1

Excession of blade's power consumption
Exceeding the maximum combined power dissipation of installed PMC modules may damage the blade.
Make sure that the combined power dissipation of installed PMC modules on the 3.3V and 5V rail does not exceed 60W.

PMC Module Malfunctioning
Processor PMC modules (as defined in ANSI/VITA 32–2003) can be operated in two different modes: monarch and non–monarch mode.
Make sure to operate any installed processor PMC modules (as defined in ANSI/VITA 32–2003) only in non–monarch mode.

Damage of Installed Hard Disk
If PPMC/270 or PPMC/280 modules are installed into PMC slot 1 or 2, the heat radiated by the heat sink of theses PMC modules heats up an installed hard disk that may be installed at the same time.
If PPMC/270 or PPMC/280 modules are installed into PMC slot 1 or 2, make sure not to have a hard disk installed at the same time.

Battery

Blade/System damage
Incorrect exchange of lithium batteries can result in a hazardous explosion.
Therefore, exchange the battery as described in this manual.

Data loss
If the battery does not provide enough power anymore, the RTC is initialized and the data in the NVRAM is lost.
Therefore, exchange the battery before seven years of actual battery use have elapsed.

Data loss
Exchanging the battery always results in data loss of the devices which use the battery as power backup.
Therefore, back up affected data before exchanging the battery.

Data loss
If installing another battery type than is mounted at blade delivery may cause data loss since other battery types may be specified for other environments or may have a shorter lifetime.
Therefore, only use the same type of lithium battery as is already installed.

Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, die bei Installation, Betrieb und Wartung des Produkts zu beachten sind.

Wir sind darauf bedacht, alle notwendigen Informationen, die für die Installation und den Betrieb erforderlich sind, in diesem Handbuch bereit zu stellen. Da es sich jedoch um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Motorola.

Das Produkt erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.

Installation, Wartung und Betrieb dürfen nur von durch Motorola ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können es aber in keinem Fall ersetzen.

EMV

Das Blade wurde in einem Motorola Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC–Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Blades in Gewerbe– sowie Industriegebieten gewährleisten.

Das Blade arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

Installation

Beschädigung von Schaltkreisen
Elektrostatische Entladung und unsachgemäßer Ein– und Ausbau von Blades kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.
Bevor Sie Blades oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD–geschützten Bereich arbeiten.

Datenverlust
Wenn Sie das Blade aus dem Shelf herausziehen, und die blaue LED blinkt noch, gehen Daten verloren.
Warten Sie bis die blaue LED durchgehend leuchtet, bevor Sie das Blade herausziehen.

Beschädigung des Blades und von Zusatzmodulen
Fehlerhafte Installation von Zusatzmodulen, kann zur Beschädigung des Blades und der Zusatzmodule führen.
Lesen Sie daher vor der Installation von Zusatzmodulen die zugehörige Dokumentation.

Betrieb

Beschädigung des Blades
Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Blades können zu Kurzschlüssen führen.
Betreiben Sie das Blade nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Blade kein Kondensat befindet und betreiben Sie das Blade nicht unter 0˚C.

Überhitzung und Beschädigung des Blades
Betreiben Sie das Blade ohne Zwangsbelüftung, kann das Blade überhitzt und schließlich beschädigt werden.
Bevor Sie das Blade betreiben, müssen Sie sicher stellen, dass das Shelf über eine Zwangskühlung verfügt.

Wenn Sie das Blade in Gebieten mit starker elektromagnetischer Strahlung betreiben, stellen Sie sicher, dass das Blade mit dem System verschraubt ist und das System durch ein Gehäuse abgeschirmt wird.

Verletzungen oder Kurzschlüsse
Blade oder Stromversorgung
Falls die ORing Dioden des Blades durchbrennen, kann das Blade einen Kurzschluss zwischen den Eingangsleitungen A und B verursachen. In diesem Fall ist Leitung A immer noch unter Spannung, auch wenn sie vom Versorgungskreislauf getrennt ist (und umgekehrt).
Prüfen Sie deshalb immer, ob die Leitung spannungsfrei ist, bevor Sie Ihre Arbeit fortsetzen, um Schäden oder Verletzungen zu vermeiden.

Schaltereinstellungen

Fehlfunktion des Blades
Schalter, die mit 'Reserved' gekennzeichnet sind, können mit produktionsrelevanten Funktionen belegt sein. Das Ändern dieser Schalter kann im normalen Betrieb Störungen auslösen.
Verstellen Sie nur solche Schalter, die nicht mit 'Reserved' gekennzeichnet sind.
Prüfen und ändern Sie die Einstellungen der nicht mit 'Reserved' gekennzeichneten Schalter, bevor Sie das Blade installieren.

Beschädigung der Blade
Das Verstellen von Schaltern während des laufenden Betriebes kann zur Beschädigung des Blades führen.
Prüfen und ändern Sie die Schaltereinstellungen, bevor Sie das Blade installieren.

Umweltschutz

Entsorgen Sie alte Batterien und/oder Blades stets gemäß der in Ihrem Land gültigen Gesetzgebung, wenn möglich immer umweltfreundlich.

PMC–Module

Begrenzte Leistung auf dem PMC–Modul und RTM
Das Blade verfuegt ueber keine Sicherung fuer PMC–Module und RTMs.
PMC–Module und RTMs, die zusammen mit dem Blade eingesetzt werden, muessen gemaess den folgenden Standards qualifiziert sein: IEC 60950–1, EN 60950–1, UL 60950–1, CAN/CSA C22–2 No 60950–1

Ueberschreitung der zulaessigen Leistungsaufnahme des Blades
Wird die maximal zulaessige Leistungsaufnahme fuer alle installierten PMC–Module zusammen ueberschritten, so kann dies zu einer Beschaedigung des Blades fuehren.
Stellen Sie sicher, dass die Leistungsaufnahme aller installierten PMC–Module zusammen auf der 3.3V– und 5V–Schiene insgesamt 60W nicht ueberschreitet.

Fehlfunktion von PMC–Modulen
Prozessor–PMC–Module (ANSI/VITA 32–2003) koennen generell in zwei Modi betrieben werden: Monarch– und Nonmonarch–Modus.
Betreiben Sie auf dem Blade installierte PMC–Module (ANSI/VITA 32–2003) nur im Nonmonarch–Modus.

Beschaedigung einer installierten Festplatte
Falls PPMC/270 oder PPMC/280-PMC-Module in PMC-Slot 1 oder 2 installiert sind, erhitzen die Kuehlkoerper dieser PMC-Module eine moeglicherweise gleichzeitig installierte Festplatte.
Falls PPMC/270- oder PPMC/280-PMC-Module in den PMC-Slots 1 oder 2 installiert sind, stellen Sie sicher, dass keine Festplatte zur gleichen Zeit auf dem Blade installiert ist.

Batterie

Beschaedigung des Blades/des Systems
Fehlerhafter Austausch von Lithium-Batterien kann zu gefährlichen Explosionen führen.
Fuehren Sie den Austausch so durch, wie er in diesem Manual beschrieben ist.

Datenverlust
Wenn die Batterie nur noch ungenügend geladen ist, wird der RTC zurückgesetzt und Daten im NVRAM gehen verloren.
Tauschen Sie daher die Batterie innerhalb einer Zeit von spätestens sieben Jahren aus.

Datenverlust
Der Austausch der Batterie führt unweigerlich zu Datenverlust bei Bauteilen, die die Batterie als Backup verwenden.
Sichern Sie daher alle Daten, die bei Austausch der Batterie verloren gehen.

Datenverlust
Wenn Sie einen anderen Batterietyp installieren als der, der bei Auslieferung des Blades installiert war, kann Datenverlust die Folge sein, da die neu installierte Batterie für andere Umgebungsbedingungen oder eine andere Lebenszeit ausgelegt sein könnte.
Verwenden Sie daher den gleichen Batterietyp, der bei Auslieferung des Blades installiert war.

1

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About this Manual

This Reference Guide provides the information you need to install, access and operate the blade.

Organization of this Manual

The Reference Guide is organized as follows.

Table 1: *Organization of this Manual*

Chapter	Description
Using this Guide	Lists all conventions and abbreviations used in this manual and outlines the revision history
Other Sources of Information	Lists related documentation and specifications
Safety Notes	Provides safety relevant information when handling the product
Sicherheitshinweise	German translation of the Safety Notes section
Introduction	Provides a basic overview of the features of the product and this manual
Installation	Outlines the installation requirements, hardware accessories, switch settings, installation and removal procedures
Controls, Indicators and Connectors	Describes the LEDs, keys, and connectors of the product
BIOS	Describes the basic features of the blade's BIOS. Also explains how to restore the BIOS default settings and how to connect to the blade using the serial console redirect feature.
Devices' Features and Data Paths	Provides detailled information on the devices, such as controllers, CPU etc., used on the blade and how they are interconnected
Maps and Registers	Provides information that is relevant for programmers, such as register reference and memory maps
Battery Exchange	Describes how to exchange the blade's on-board battery

Feedback

Motorola welcomes and appreciates your comments on its documentation. We want to know what you think about our manuals and how we can make them better. Mail comments to:

- Motorola GmbH
  ECC Embedded Communication Computing
  Lilienthalstr. 15
  85579 Neubiberg-Munich/Germany

- reader–comments@mcg.mot.com

In all your correspondence, please list your name, position, and company. Be sure to include the title, part number, and revision of the manual and tell how you used it.

Features

The PENT/ATCA-717 is an AdvancedTCA compliant single blade computer offering high processing performance. Four on-board PMC sites, GBit Ethernet connection to the AdvancedTCA Base and Fabric interface as well as standard I/O interfaces make it ideal for telecommunication and datacom applications. An on-board 16-port Ethernet switch allows switching between PMC sites, Base and Fabric interface and the base board.

Important features are:

- Pentium M processor with up to 1.8 GHz speed
- Up to four GByte main memory DDR2 SDRAM with ECC protection
- Designed for PICMG 3.0 and 3.1 compliant systems
- 16-port Ethernet switch with host interface for configuration and management
- Redundant AdvancedTCA Base interface
- Up to eight AdvancedTCA Fabric Channel interfaces
- Four 64-bit/100MHz PCI-X compliant PMC slots
- Two USB 2.0 interfaces at face plate
- Optional on-board CompactFlash and 2.5 inch hard disk
- Support for Windows 2000/2003 and Carrier Grade Linux Ed. 3.1
- Intelligent Platform Management Controller (IPMC) compliant to IPMI V.1.5 with redundant IPMB support
- Support for four PMC Modules with Telecom clocking synchronization
- Different accessory kits, for example:
  - Rear Transition Modules (RTMs)
  - CMC debug module
  - Hard disk accessory kit
  - Cable accessory kits

Standard Compliances

Standard	Description
UL 60950–1 EN 60950–1 IEC 60950–1 CAN/CSA C22.2 No 60950–1	Legal safety requirements
EN 55022 EN 55024 EN 300386 FCC Part 15	EMC requirements on system level (predefined Motorola system)
ANSI/IPC–A610 Rev.C Class 2 ANSI/IPC–7711 ANSI/IPC–7721 ANSI–J–001...003	Manufacturing Requirements
ISO 8601	Y2K compliance
NEBS Standard GR–63–CORE, NEBS Standard GR–1089 CORE	NEBS level three Product is designed to support NEBS level three. The compliance tests must be done with the customer target system.
PICMG 3.0 R1.0	Defines mechanics, blade dimensions, power distribution, power and data connectors, and system management

Note: This blade contains an embedded power source rated >150W. To achieve NEBS compliance on system level, Shelf Ground (chassis ground) and Logic Ground (logic signal return) have to be connected. The connection may be implemented inside the shelf, e.g. at the backplane, or the shelf has to provide a possibility to lead Logic Ground out of the shelf for external connection to Central Office Ground. For further information refer to Telcordia GR–1089–CORE, section 9.8.2, requirement R9–14.

Ordering Information

When ordering the board variants, upgrades and accessories, use the order numbers given below.

Product Nomenclature

In the following you find the key for the product name extensions.

PENT/ATCA-717/xx-yyyy	
xx	Main memory in GByte
yyyy	CPU frequency in MHz

Order Numbers

The table below is an excerpt from the blade's ordering information. Ask your local Motorola representative for the current ordering information.

Note: This manual describes the blades listed below (PCA revision 1.3) and is delivered with these blades. For blades with other PCA revisions refer to the manuals that are delivered with those blades.

Table 2: *Ordering Information*

Order Number	PENT/ATCA-717/	Description
123065	2G-1800	Two GByte main memory, 1800 MHz CPU frequency; (PCA revision 1.3)
123066	4G-1800	Four GByte main memory, 1800 MHz CPU frequency; (PCA revision 1.3)

The table below is an excerpt from the blade's accessories ordering information. Ask your local Motorola representative for the current ordering information.

Table 3: *Accessories Ordering Information*

Order Number	Accessory	Description
123036	ACC/ARTM-717	Rear transition module for PENT/ATCA-717 blades Provides access to four serial interfaces deriving from PMCs as well as two USB 2.0, two serial, two SATA and one keyboard/mouse interface; supports PPMC-280 modules installed on the PENT/ATCA-717
120980	ACC/ATCA-715/HDD	Parallel ATA hard disk

Order Number	Accessory	Description
122240	ACC/ATCA-715/HDD-SATA	Serial ATA hard disk
122241	ACC/ATCA-CMC-MODULE	CMC module for debugging
121793	ACC/CABLE/RJ45/DSUB	Adapter cable: RJ-45 <-> DSUB
122242	ACC/CABLE/PMC/RJ45	Splitter cable for accessing serial interfaces of installed PMC − 8260/DS1 or PPMC − 280 modules
121792	ACC/CABLE/USB	Adapter cable: mini USB B-male <-> USB A female

2

Installation

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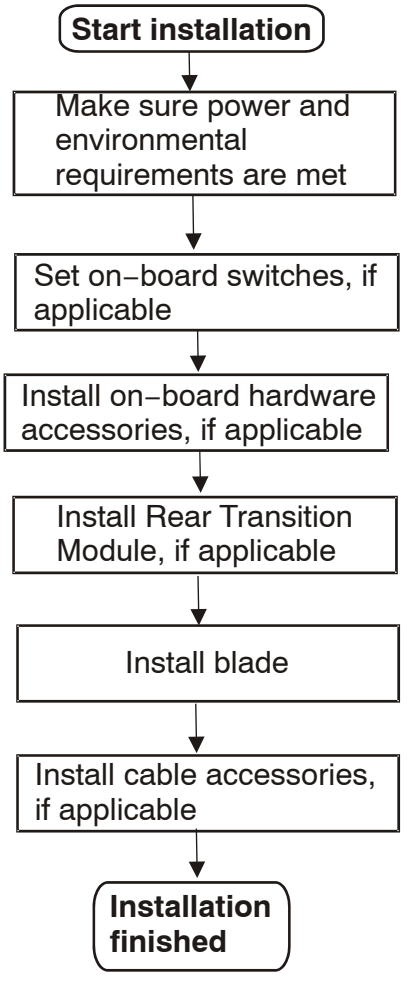
Action Plan

To install the blade, the following steps are necessary and described in detail in the sections of this chapter. The installation takes about five minutes.


Start installation
Make sure power and environmental requirements are met
Set on−board switches, if applicable
Install on−board hardware accessories, if applicable
Install Rear Transition Module, if applicable
Install blade
Install cable accessories, if applicable
Installation finished

Requirements

In order to meet the environmental requirements, the blade has to be tested in the system in which it is to be installed.

Before you power up the blade, calculate the power needed according to your combination of blade upgrades and accessories.

Environmental Requirements

The environmental conditions must be tested and proven in the shelf configuration used. The conditions refer to the surrounding of the blade within the user environment.

Note:

- **The environmental requirements of the blade may be further limited down due to installed accessories, such as hard disks or PMC modules, with more restrictive environmental requirements**
- **Operating temperatures refer to the temperature of the air circulating around the blade and not to the actual component temperature.**

Caution

- **Blade damage**
  Blade surface
  High humidity and condensation on the blade surface causes short circuits.
  Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power. Do not operate the blade below 0˚C.

- **Blade Overheating and Blade Damage**
  Operating the blade without forced air cooling may lead to blade overheating and thus blade damage.
  When operating the blade, make sure that forced air cooling is available in the shelf.

Table 4: *Environmental Requirements*

Requirement	Operating	Non-Operating
Temperature	0˚C to +55˚C (may be further limited by installed accessories)	–40˚C to +85˚C (may be further limited by installed accessories)
Temp. Change	+/– 0.5˚C/min	+/– 1˚C/min

Requirement	Operating	Non–Operating
Rel. Humidity	5% to 95% non condensing at +40˚	5% to 95% non condensing at +40˚C
Altitude	–300 m to +3,000 m	–300 m to +13,000 m
Vibration		
20 to 2000Hz	2 g(RMS) random	2 g(RMS) random
Shock	5 g/30 ms half sine	15 g/11 ms half sine
Free Fall		1,200 mm/all edges and corners (packed state) 100 mm/3 axis (unpacked)

To guarantee proper blade operation, you have to make sure that the temperatures at the following locations are not exceeded. If not stated otherwise, the temperatures should be measured by placing a sensor exactly at the given locations.

Location No.	Component	Temperature Limit
1	Pentium M CPU [1)]	100 ˚C
2	Intel 82540EM Gbit Ethernet controller	100 ˚C
3	Intel 6300ESB Southbridge	105 ˚C
4	Lithium battery	70 ˚C
5	Intel 82546EB/GB Dual Gbit Ethernet controller	90 ˚C
6	Electrolytic capacitor CE9902	100 ˚C
7	Electrolytic capacitor CE9903	100 ˚C
8	Ericsson DC/DC converter	90 ˚C
9	QM48T DC/DC converter	115 ˚C (105 ˚C coated blade variant)
10	Power MOSFET IRF 6603	105 ˚C

1) Temperature must be measured via on–die sensor which can be accessed via IPMI

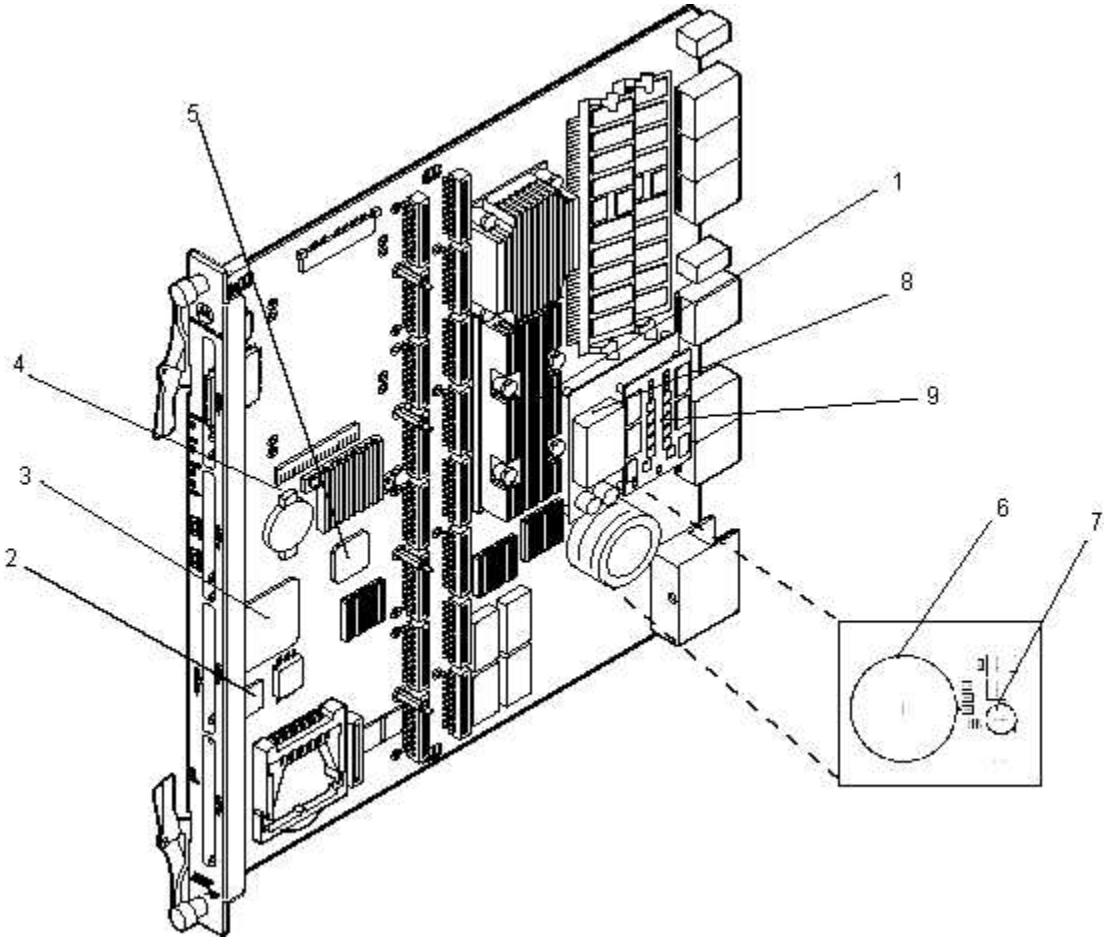


Figure 1: *Location of Critical Blade Temperature Spots (Blade Top Side)*

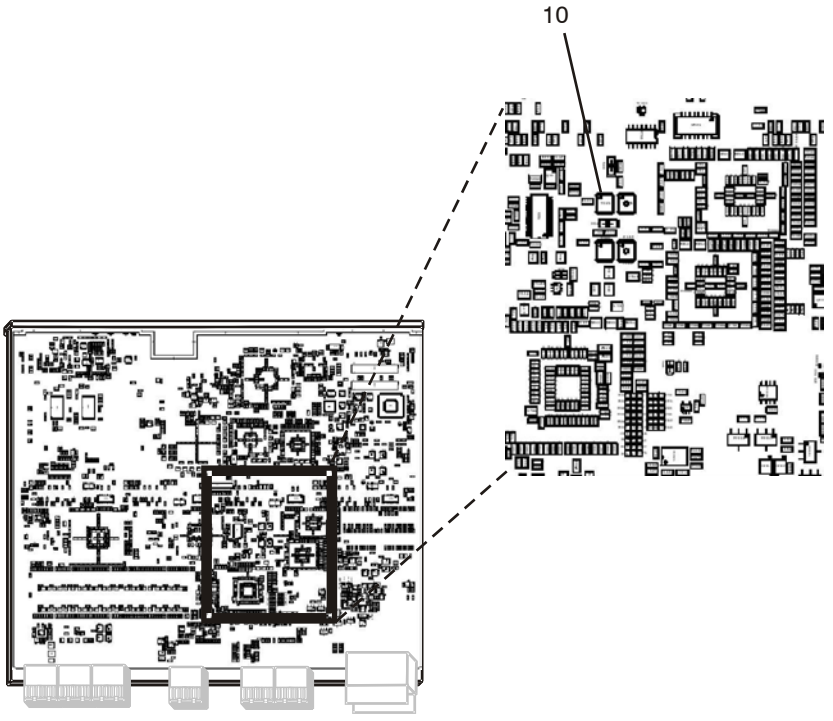


Figure 2: *Location of Critical Blade Temperature Spots (Blade Bottom Side)*

Power Consumption

The blade's power requirements depend on the installed hardware accessories. If you want to install accessories on the board, the load of the respective accessory has to be added to that of the blade.In the following table you will find typical examples of power requirements with and without accessories installed. For information on the accessories' power requirements, refer to the documentation delivered together with the respective accessory or consult your local Motorola representative for further details.

The blade must be connected to a TNV-2 or a safety-extra-low-voltage (SELV) circuit. A TNV-2 circuit is a circuit whose normal operating voltages exceed the limits for a SELV circuit under normal operating conditions, and which is not subject to overvoltages from telecommunication networks.

Table 5: *Power Requirements*

Characteristic	Value
Rated Voltage Exception in the US and Canada	-48VDC to -60VDC -48VDC
Operating Voltage Exception in the US and Canada	-40.5VDC to -72VDC -40.5VDC to -60VDC

Characteristic	Value
Max. current	3.6A
Max. power consumption of blade equipped with 4 GByte SDRAM without accessories	75W
Max. total power consumption of all four PMC sites	60W
Max. total power consumption of all installed blade accessories (PMCs + hard disk)	65W

The blade provides two independent power inputs according to the AdvancedTCA Specification. Each input has to be equipped with an additional fuse of max. 90A located either in the shelf where the blade is installed or the power entry module (PEM).

Switch Settings

The blade provides the on-board switches SW2, SW3, SW4 and SW7. The following figure shows their location. Note that in the switch drawings the switch handle is represented by a little white square and that the shown switch settings reflect the default switch settings.

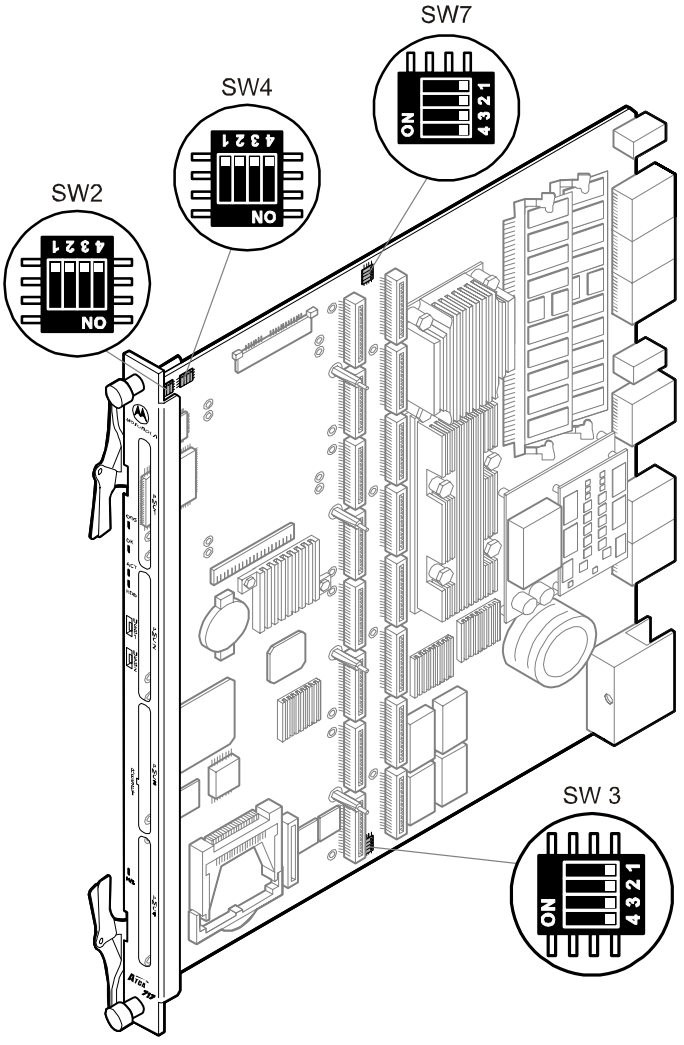


Figure 3: *Location of On-board Switches*

Caution

- **Blade Malfunction**
  Switches marked as 'reserved' might carry production–related functions and can cause the blade to malfunction if their setting is changed.
  Therefore, do not change settings of switches marked as 'reserved'. The setting of switches which are not marked as 'reserved' has to be checked and changed before blade installation.

- **Blade Damage**
  Setting/resetting the switches during operation can cause blade damage.
  Therefore, check and change switch settings before you install the blade.

Table 6: *Switch Settings*

Switch	Description
SW2–1	Reserved (default: OFF)
SW2–2	Reserved (default: OFF)
SW2–3	Clear CMOS RAM content OFF: Normal operation (default) ON: Clear CMOS RAM For the exact procedure of how to clear the CMOS RAM content, i.e. restore the default BIOS settings, refer to section "Restoring BIOS Default Settings" on page 91.
SW2–4	BIOS crisis recovery mode OFF: Disabled (default) ON: Enabled For details refer to section "BIOS Crisis Recovery Mode" on page 86.
SW3–1	Reserved (default: OFF)
SW3–2	Reserved (default: OFF)
SW3–3	Reserved (default: OFF)
SW3–4	Serial COM interface swapping at blade start–up OFF: No swapping (default) As a result, COM1 and COM2 are accessible at an installed RTM, COM3 and COM4 are accessible at an installed CMC module ON: COM1 is swapped with COM 3, and COM 2 is swapped with COM 4 As a result, COM1 and COM2 are accessible at an installed CMC module, and COM3 and COM4 are accessible at an installed RTM

Switch	Description
	Note: the routing described above is only applicable to BIOS versions ≥ 2.0.0. Earlier BIOS versions used a different routing. For further information refer to the *PENT/ATCA-715/717/7105/7107 BIOS Information Sheet* which can be downloaded from the former Force Computers S.M.A.R.T. server or the Motorola literature catalog web site. **Note**: The COM port swapping can also be enabled via a System Boot Option IPMI command. COM port swapping is enabled if either the switch or the IPMI command or both enable it. For further details about the System Boot Option IPMI command, refer to the *PENT/ATCA-715/717/7105/7107: Control via IPMI Programmer's Guide*.
SW4-1	Backup boot flash boot block write protection OFF: Write-enabled (default) ON: Write-disabled For details on the flash devices and the blade's redundant BIOS feature, refer to section "Flash Devices" on page 113.
SW4-2	Default boot flash boot block write protection OFF: Write-enabled (default) ON: Write-disabled For details on the flash devices and the blade's redundant BIOS feature, refer to section "Flash Devices" on page 113.
SW4-3	Reserved (default: OFF)
SW4-4	Backup boot flash data/instruction block write protection OFF: Write-enabled (default) ON: Write-disabled For details on the flash devices and the blade's redundant BIOS feature, refer to section "Flash Devices" on page 113.
SW7-1	Routing of PMC slot 1 Pn4 connector pins 30 and 31 OFF: Pin 30 and 31 are routed to zone 3 backplane connector and are available as PMC I/O signals (default) ON: Pin 30 and 31 hold clock reference signals generated by clock synchronization building block
SW7-2	Routing of PMC slot 2 Pn4 connector pins 30 and 31 OFF: Pin 30 and 31 are routed to zone 3 backplane connector and are available as PMC I/O signals (default) ON: Pin 30 and 31 hold clock reference signals generated by clock synchronization building block

Switch	Description
SW7–3	Routing of PMC slot 3 Pn4 connector pins 30 and 31 OFF: Pin 30 and 31 are routed to zone 3 backplane connector and are available as PMC I/O signals (default) ON: Pin 30 and 31 hold clock reference signals generated by clock synchronization building block
SW7–4	Routing of PMC slot 4 Pn4 connector pins 30 and 31 OFF: Pin 30 and 31 are routed to zone 3 backplane connector and are available as PMC I/O signals (default) ON: Pin 30 and 31 hold clock reference signals generated by clock synchronization building block

On–Board Hardware Accessories

The following hardware upgrades can be installed on the blade:

- PMC modules
- Hard Disk
- CompactFlash card
- CMC module

PMC Modules

The blade provides four PMC slots supporting PCI/PCI–X based PMC modules. When operated in PCI mode, PMC modules run at 33/66Mhz, when operated in PCI–X mode they run at 66/100MHz. All four PMC slots use a signaling level of 3.3V.

The four PMC slots are numbered from 1 to 4. Their location is shown in the following figure.

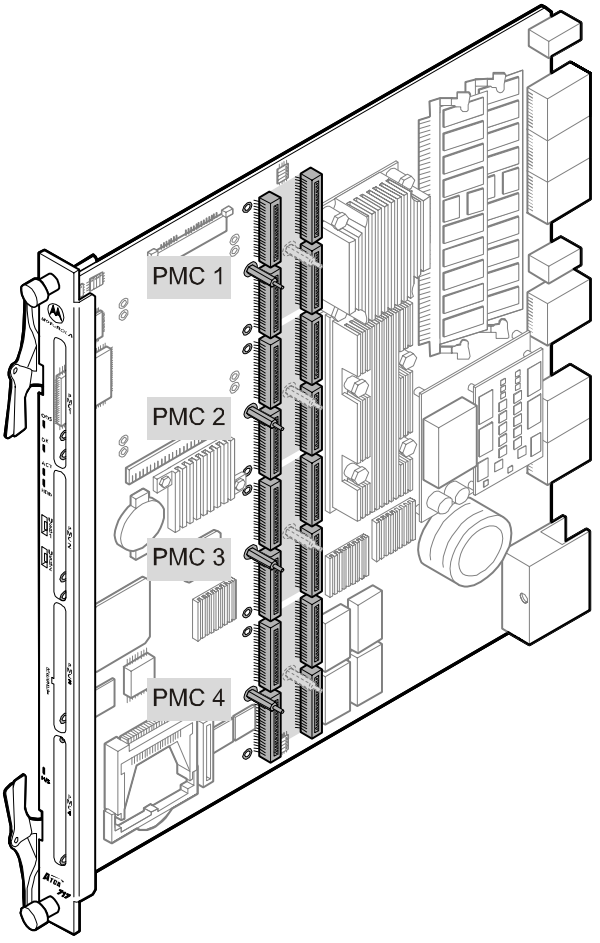


Figure 4: *Location of PMC Slots*

PMC slots 1 and 2 belong to one PCI segment and PMC slots 3 and 4 belong to another PCI segment. Within the same PCI segment, it is possible to install two PMC modules of different modes (PCI/PCI–X) and speeds (33/66/100 MHz). The PMC module with the overall lower performance (combination of speed and PCI mode) determines the speed and PCI mode of the second PMC module.

Example: A PMC module supporting PCI–X/66MHz is installed into PMC slot 1 and a PMC module supporting PCI/66MHz is installed into PMC slot 2. In this case both PMC modules are operated in PCI/66 MHz mode because the PMC module with the overall less performance is the one supporting PCI/66 MHz and consequently the second PMC module is operated in this mode as well.

Before installing PMC modules, the following general safety notes must be observed.

- **Limited Power on PMC Modules and RTMs**
  The blade does not provide an extra fuse for PMC modules and RTMs.
  PMC modules and RTMs used together with the blade have to be qualified according to the following standards: IEC 60950–1, EN 60950–1, UL 60950–1, CAN/CSA C22–2 No 60950–1

- **Excession of blade's power consumption**
  Exceeding the maximum combined power dissipation of installed PMC modules may damage the blade.
  Make sure that the combined power dissipation of installed PMC modules on the 3.3V and 5V rail does not exceed 60W.

- **PMC Module Malfunctioning**
  Processor PMC modules (as defined in ANSI/VITA 32–2003) can be operated in two different modes: monarch and non–monarch mode.
  Make sure to operate any installed processor PMC modules (as defined in ANSI/VITA 32–2003) only in non–monarch mode.

- **Damage of Installed Hard Disk**
  If PPMC/270 or PPMC/280 modules are installed into PMC slot 1 or 2, the heat radiated by the heat sink of theses PMC modules heats up an installed hard disk that may be installed at the same time.
  If PPMC/270 or PPMC/280 modules are installed into PMC slot 1 or 2, make sure not to have a hard disk installed at the same time.

- **Damage of Rear Transition Module and Blade**
  The ACC/ARTM–717 was designed to be used in conjunction with PPMC/270 or PPMC/280 modules modules installed on the blade at the same time.
  In order to avoid damage of the blade or RTM, only use the ACC/ARTM–717 in conjunction with PPMC/270 or PPMC/280 modules.

Installation Procedure

1. Connect PMC module carefully to PMC slot
2. Make sure that 15 mm standoffs of PMC module cover mounting holes of the blade.
3. Place screws delivered with PMC module into mounting holes
4. Fasten screws

Removal Procedure

1. Remove screws
2. Disconnect PMC module carefully from slot

Hard Disk

The blade allows to install one 2.5″ hard disk which may be connected to either an on–board parallel or serial Advanced Technology Attachment (ATA) interface connector. The hard disk can be mounted directly on the blade without the need for an additional wire.

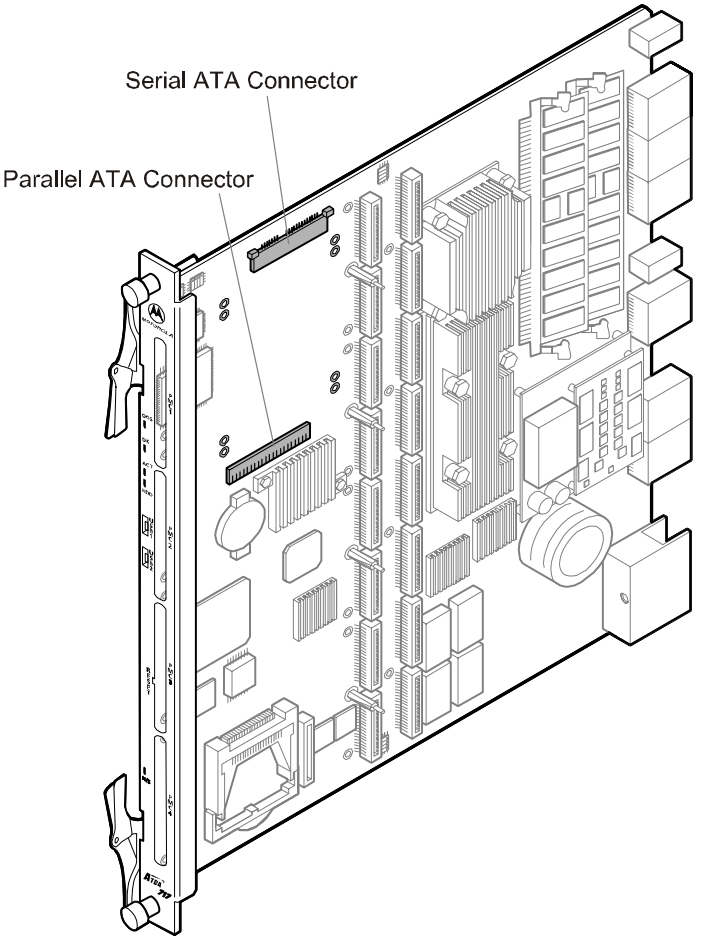


Figure 5: *Location of On–Board Hard Disk*

The serial ATA interface supports up to 150 MByte/s data transfer rate and the parallel ATA supports all PIO and DMA modes up to Ultra ATA100. Hard disks which are connected to the parallel ATA interface act as master.

Two hard disk accessory kits are available for the blade. One is called ACC/ATCA–715/HDD and contains a parallel ATA hard disk drive. The second is called ACC/ATCA–715/HDD–SATA and contains a serial ATA hard disk drive.

Installing a Hard Disk

1. Position hard disk above blade so that the blade′s parallel ATA or serial ATA or SATA connector faces the hard disk′s interface connector
2. Connect hard disk with blade′s connector
3. Turn blade to face its bottom side
4. Fasten four screws to blade′s bottom side

Removing a Hard Disk

1. Removing Hard Disk
2. Place blade on table with blade′s bottom side facing you
3. Remove four screws holding hard disk
4. Carefully remove hard disk from blades′s parallel ATA or SATA connector
5. Store hard disk and screws in a safe place in case you want to use the accessory kit components again

CompactFlash Disk

The blade provides a connector to install a CompactFlash card of type I and II.

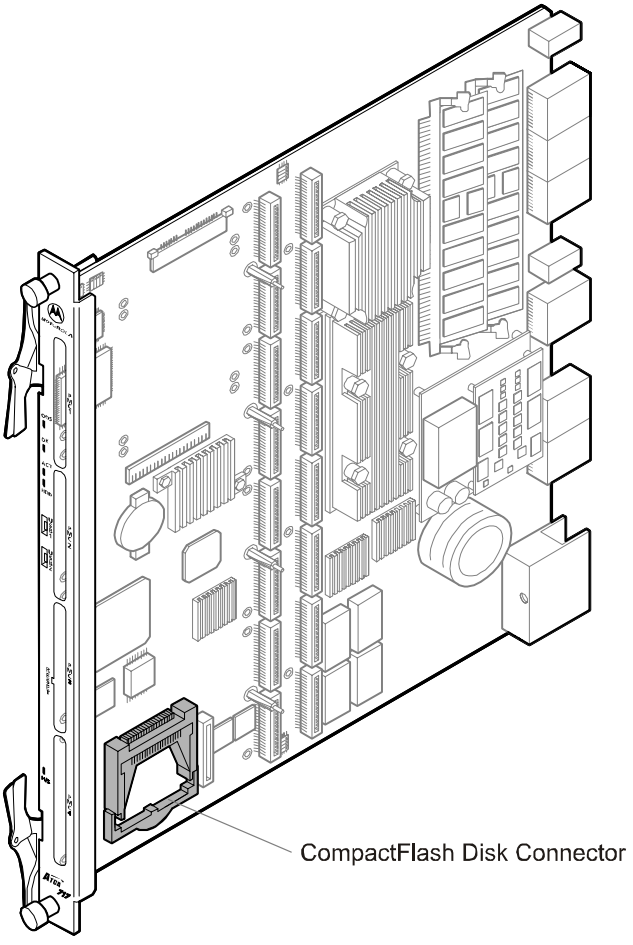
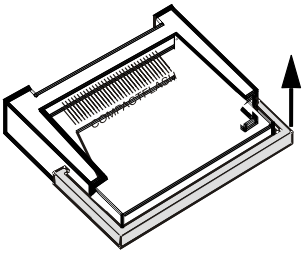


Figure 6: *Location of CompactFlash Disk Connector*

The CompactFlash card is operated in True IDE mode and is connected to the secondary IDE interface where it acts as IDE master.

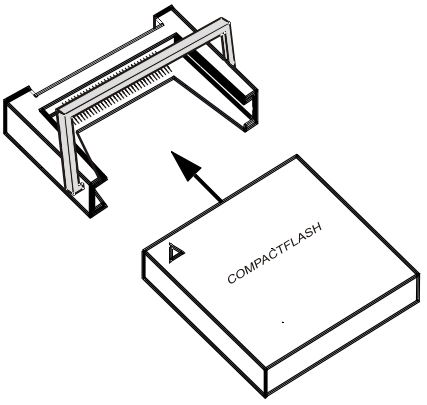
CompactFlash Installation

1. Open locking bow

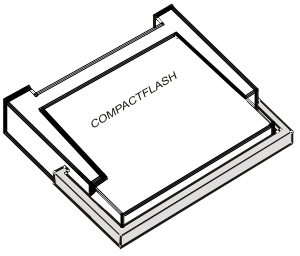


2. Check that disk's connectors face the CompactFlash socket

3. Plug CompactFlash into socket



4. Close locking bow over CompactFlash disk



Note: The locking bow must enclose the disk completely.

Removal Procedure

1. Open locking bow
2. Take CompactFlash disk's ends and pull CompactFlash disk carefully out of socket
3. Close locking bow again

CMC Debug Module

A CMC debug module is available as accessory kit for the blade. It is called ACC/ATCA-CMC-MODULE and provides two serial and one keyboard/mouse interface at its face plate. The CMC debug module is installed into PMC slot 4. For further details refer to the *ACC/ATCA-CMC-MODULE Installation Guide*.

Rear Transition Modules

At the time of writing this manual the following Rear Transition Modules (RTMs) was available for the blade: ACC/ARTM–717

It provides the following interfaces:

- Two USB 2.0
- Two RS–232
- Keyboard/Mouse
- One serial ATA
- Four RS–232 interfaces routed from PMC modules installed on the base blade

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Note:

- **Refer to the RTM documentation for the RTM installation procedure**
- **Check the documentation of the system where you operate the blade and the RTM for any restrictions that may apply to the blade or the RTM**
- **No hot–swap is supported for the RTMs**

The RTM furthermore incorporates an Intelligent Platform Management Interface Controller (IPMC) which enables you to monitor the RTM's temperature and voltage sensors. For further information, refer to the *ACC/ARTM–715/717/7105/7107: Control via IPMI Programmer's Guide* which can be downloaded from the former Force Computers S.M.A.R.T. server or the Motorola literature catalog.

Blade Installation

The blade is fully compatible to the AdvancedTCA standard and is designed to be used in AdvancedTCA shelfs. Since the installation and removal procedures are different for powered and nonpowered shelfs, they are described in separate sections.

Caution

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD–safe environment.

Installation into Powered Shelves

Installation Procedure

1. Ensure that the top and bottom ejector handles are in the outward position
2. Insert blade into the shelf by placing the top and bottom edges of the blade in the card guides of the shelf. Ensure that the guiding module of shelf and blade are aligned properly.
3. Carefully slide the blade into the shelf until you feel resistance.
   If an RTM is already installed in the same slot, be careful not to bend any pins of the P30 to P32 backplane connectors.
4. Hook the lower and the upper handle into the shelf rail recesses
5. Fully insert the blade and lock it to the shelf by pressing the two components of the lower and the upper handles together and turning the handles towards the face plate
   As soon as the blade is connected to the backplane power pins, the blue LED is illuminated.
   When the blade is completely installed, the blue LED starts to blink. This indicates that the blade announces its presence to the shelf management controller.

Note: If an ARTM is connected to the front blade, make sure that the handles of both the ARTM and the front blade are closed in order to power up the blade's payload.

---

6. Wait until the blue LED is switched OFF
   The switched off blue LED indicates that the blade's payload has been powered up and that the blade is active.

7. Tighten the face plate screws which secure the blade to the shelf
8. Connect cables to the face plate, if applicable

Removal Procedure

1. Remove face plate cables, if applicable
2. Unfasten the screws of face plate until the blade is detached from shelf
3. Open the lower and the upper handle by pressing the two handle components together and turning the handles outward
   The blue LED blinks indicating that the blade power-down process is on-going.
4. Wait until the blue LED is illuminated permanently
   Note: if the LED continues to blink, a possible reason may be that upper layer software rejects the blade extraction request.

Data loss
Removing the blade with the blue LED still blinking causes data loss.
Wait until the blue LED is permanently illuminated, before removing the blade.

5. Remove the blade from the shelf

Installation in Nonpowered Shelves

Installation Procedure

1. Power down the shelf
2. Ensure that the top and botton ejector handles are in the outward position
3. Insert blade into the shelf by placing the top and bottom edges of the blade in the card guides of the shelf. Ensure that the guiding module of shelf and blade are aligned properly.
4. Slide the blade into the shelf until you feel resistance
   If an RTM is already installed in the same slot, be careful not to bend any pins of the P30 to P32 backplane connectors.
5. Hook the lower and upper handle into the shelf rail recessed
6. Fully insert the blade and lock it to the shelf by pressing the two components of the lower and upper handles together and turning the handles towards the face plate

7. Tighten the face plate screws which secure the blade to the shelf.
8. Connect cables to the face plate, if applicable

Removal Procedure

1. Remove face plate cables, if applicable
2. Unfasten the screws of the face plate until the blade is detached from the shelf
3. Open the lower and the upper handle by pressing the two handle components together and turning the handles outward
4. Remove the blade from the shelf

Cable Accessory Kits

At the time of writing this manual the following cable accessory kits are available:

- ACC/CABLE/PMC/RJ-45
- ACC/CABLE/RJ45/DSUB
- ACC/CABLE/USB

Note: Check with your local Motorola representative for the availability of further accessory kits.

ACC/CABLE/PMC/RJ–45

The ACC/CABLE/PMC/RJ45 is an accessory kit compiled for the ACC/ARTM–717 rear transition module. It contains a splitter cable which allows to access the serial interfaces of PPMC–280 modules installed on the front blade via the ARTM–717 face plate.

ACC/CABLE/RJ45/DSUB

The ACC/CABLE/RJ45/DSUB/5E is an accessory kit containing a shielded cable of 2m length and an RJ–45/DSUB adapter plug. The cable provides Null–modem functionality which enables you to connect a laptop to the serial interface of the blade. The cable can be connected to either an installed CMC module or RTM.

ACC/CABLE/USB

The ACC/CABLE/USB/5E is an USB adapter cable of 200 mm length which converts the mini USB face plate connectors to USB A female.

3

Controls, Indicators, and Connectors

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Face Plate

The following figure shows the connectors, keys and LEDs available on the face plate.

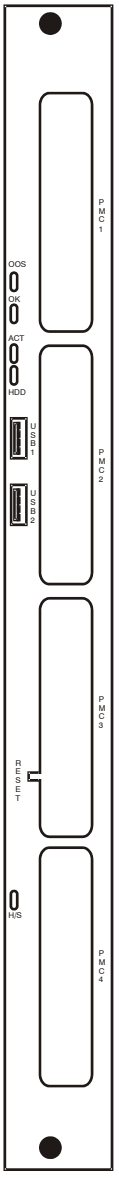


Figure 7: *Face Plate*

LEDs

The following figure shows all LEDs available at the face plate.

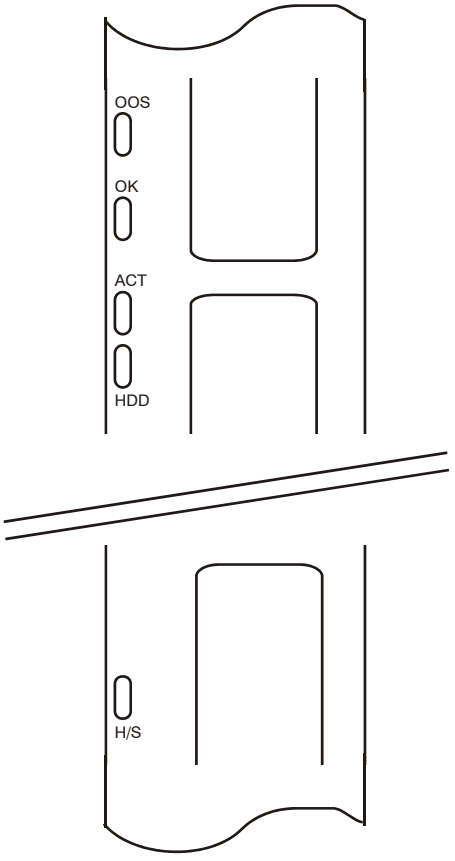


Figure 8: *Location of Face Plate LEDs*

The meaning of these LEDs is described in the following table.

Table 7: *Face Plate LEDs*

LED	Description
OOS	Out Of Service Red: Blade out of service OFF: Blade working properly
OK	Payload power status Green: Supply voltages are within threshold values OFF: Supply voltages are outside threshold values
ACT	Redundancy status Amber: Blade is active OFF: Blade is stand–by

LED	Description
HDD	**After power-up or reset** If no valid BIOS image has been found, the LED is lit red and the blade enters into BIOS crisis recovery mode. Note that the enterring into BIOS crisis recovery mode can also be enforced via the on-board switch SW2-4. For further details about the BIOS crisis recovery mode, refer to section "BIOS Crisis Recovery Mode" on page 86. **During booting** During booting this LED indicates the boot status. For each task the BIOS POST executes, the LED is toggled between red and green. **During normal blade operation:** Now the LED indicates the combined parallel/serial ATA activity or is used as user LED. Toggling between both modes is done via the LED control register In user mode: Depending on the FPGA LED control register, the LED is either red, green or OFF. In parallel/serial ATA activity mode: Green: Combined activity of parallel and serial ATA interfaces. OFF: No activity
H/S	FRU State Machine **During blade installation** Permanently blue: On-board IPMC powers up Blinking blue: Blade communicates with shelf manager OFF: Blade is active **During blade removal** Blinking blue: Blade notifies shelf manager of its desire to deactivate Permanently blue: Blade is ready to be extracted

Keys

The blade provides one face plate reset key.

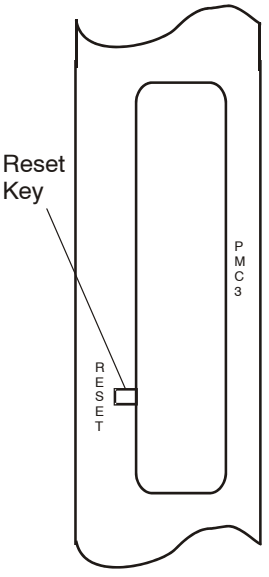


Figure 9: *Location of Reset Key*

On pressing it, a hard reset is triggered and all attached on–board devices are reset.

Note: The IPMC is not reset via this key.

Connectors

The blade provides two mini USB 2.0 connectors of type AB at its face plate. They correspond to the USB interfaces 1 and 2. An adapter cable accessory kit called ACC/CABLE/USB is available for the blade. It converts the mini USB male face plate connectors to USB female connectors.

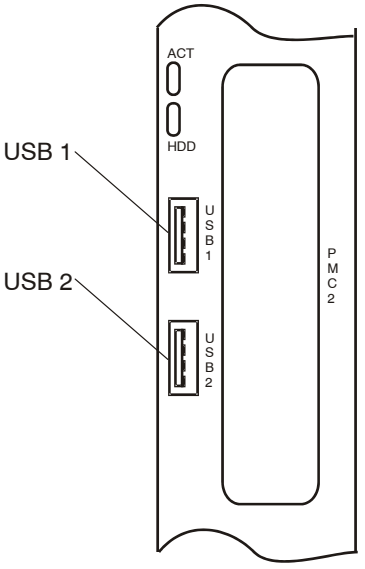


Figure 10: *Location of USB Connectors*

Their pinout is given below.

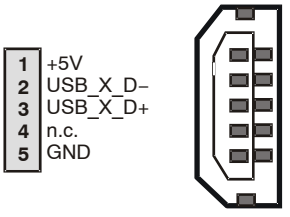


Figure 11: *Face Plate USB Connector Pinout*

On–Board Connectors

The blade provides the following on–board connectors:

- CompactFlash
- PMC
- Parallel ATA
- Serial ATA
- CMC
- ATCA backplane connectors

Note: The blade may provide further on–board connectors. These are used for debug purposes only and are therefore not documented in this guide.

CompactFlash

The CompactFlash connector is standard and is therefore not further described in this guide.

PMC

The blade provides the four PMC sites PMC#1 to PMC#4. For each PMC site the four PMC connectors Pn1 to Pn4 are provided. See the following figure.

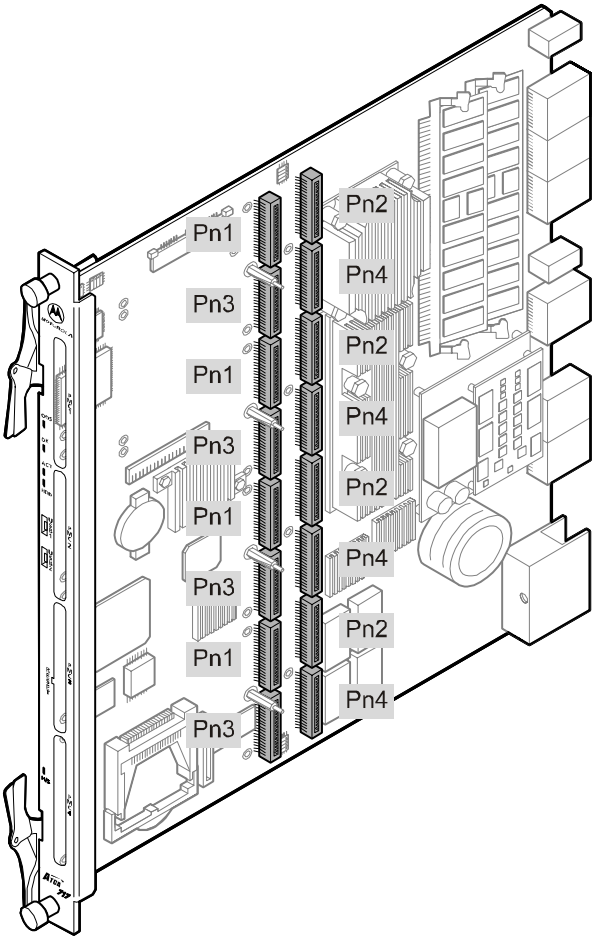


Figure 12: *Location of PMC Connectors Pn1 to Pn4*

The connectors Pn1 to Pn3 implement the PMC pinouts as specified by the IEEE P1386.1 standard. Therefore they are not documented in this guide. The connector Pn4 contains PMC I/O signals and is described in the following.

Pn4 carries the following types of signals:

- Power signals (GND)
- Clock signals (CLK_*, NETREF))
- Signals routed to on–board Ethernet switch (ETH*_)
- Signals routed to RTM (PMC_IO_*)

Part of the signals that are routed to the on–board switch and RTM (with the exception of PMC_IO_25, 26, 28, 29, 30 and 31) are grouped into length–matched differential pairs of 100 Ω impedance.

On the PMC sites 1 and 4, two Ethernet ports (signals named ETH*_) are routed to the on–board switch. On the PMC sites 2 and 3, only one port is routed to the on–board switch. The following two figures show the connector pinouts.

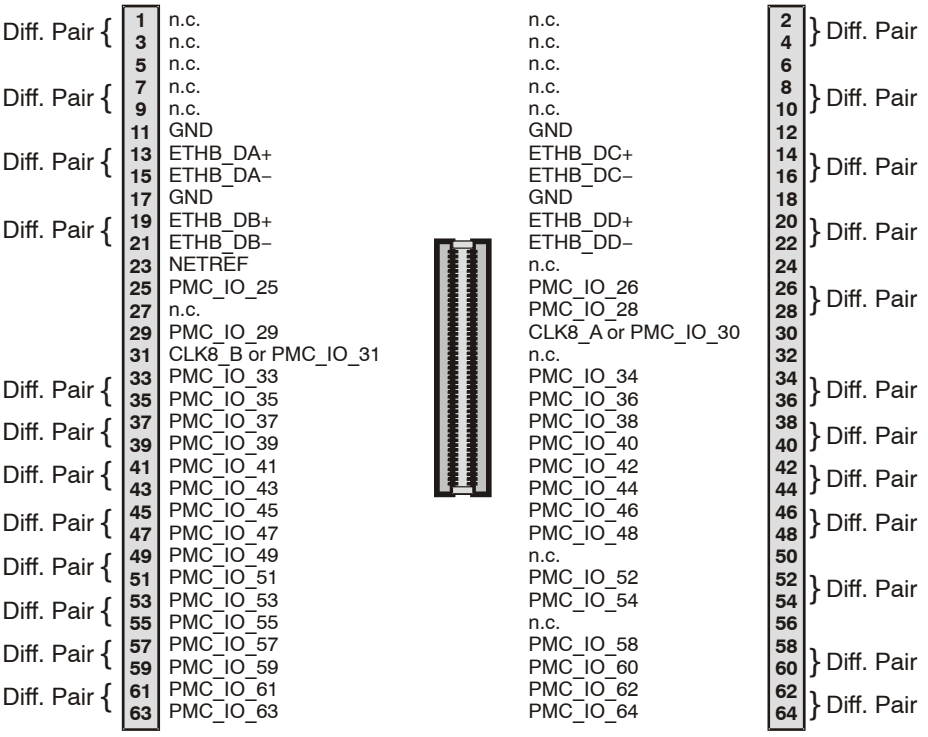


Figure 13: *PMC Sites 1 and 4 – Pn4 Connector Pinout*

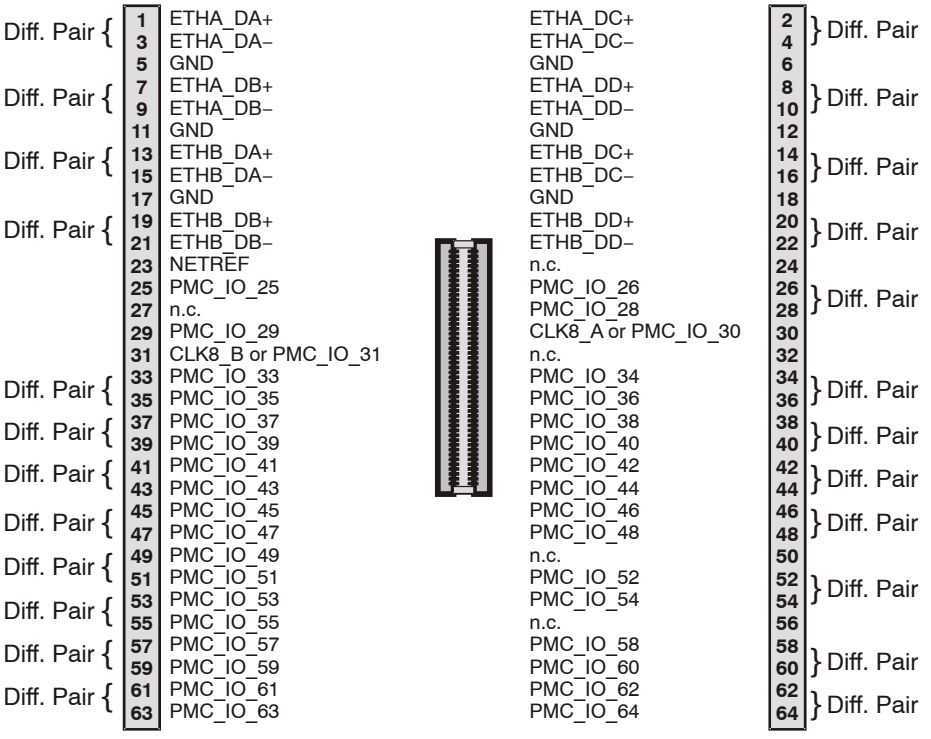


Figure 14: *PMC Sites 2 and 3 – Pn4 Connector Pinout*

Note:

- **The signals available at pins 30 and 31 depend on the settings of the on–board switches SW7–1 to SW7–4. See section ″Switch Settings″ on page 42 for further details.**
- **By default, the PMC I/O Ethernet signals (ETH_xxx) are routed to the on–board switch via magnetics. As an assembly option the magnetics can be by–passed and the Ethernet signals can be accessed via an installed PMC uplink module from Motorola. Consult your local Motorola representative for details.**
- **By default the signals at pins 61 to 64 are routed the zone 3 connectors where they are available as PMC I/O signals. As an assembly option these signals can be routed to the on–board Ethernet switch as further 100BaseTX interface. Consult your local Motorola representative for details.**

Parallel ATA Connector

The blade provides one parallel Advanced Technology Attachment (ATA) connector which allows to connect a 2.5″ hard disk to the blade. The location of this connector is shown in the following figure.

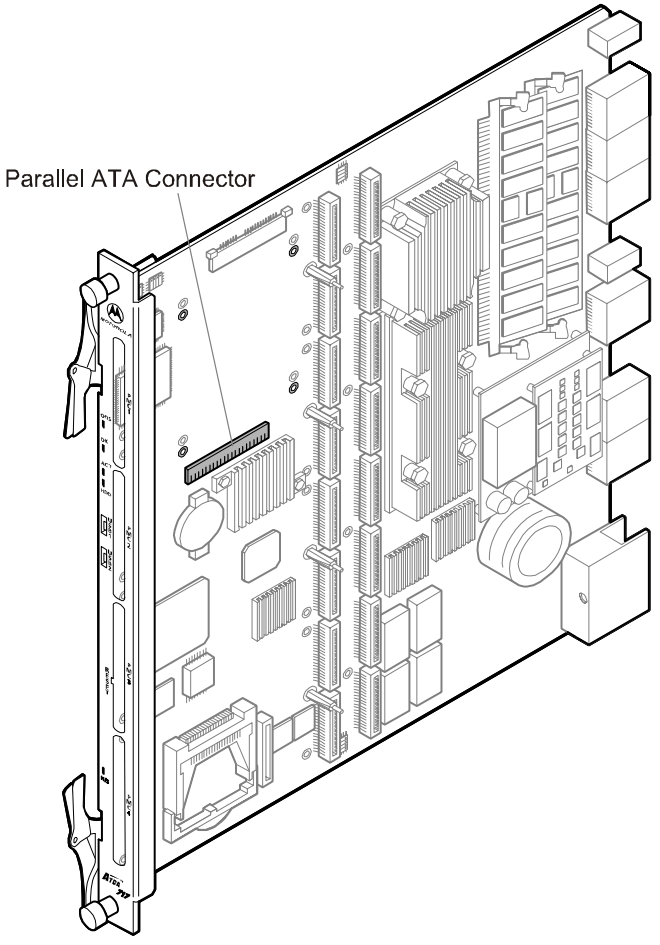


Figure 15: *Location of Parallel ATA Connector*

The pinout of the connector is as follows.

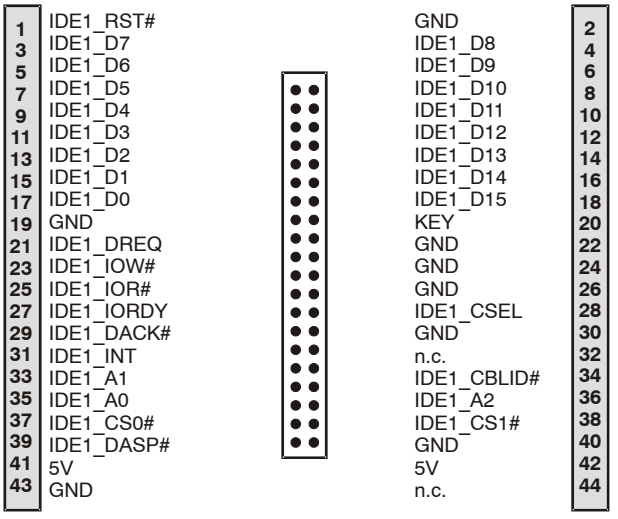


Figure 16: *Parallel ATA Connector Pinout*

Serial ATA Connector

The blade provides one Serial Advanced Technology Attachment (SATA) connector which allows to connect a hard disk to the blade. The location of the SATA connector is shown in the following figure.

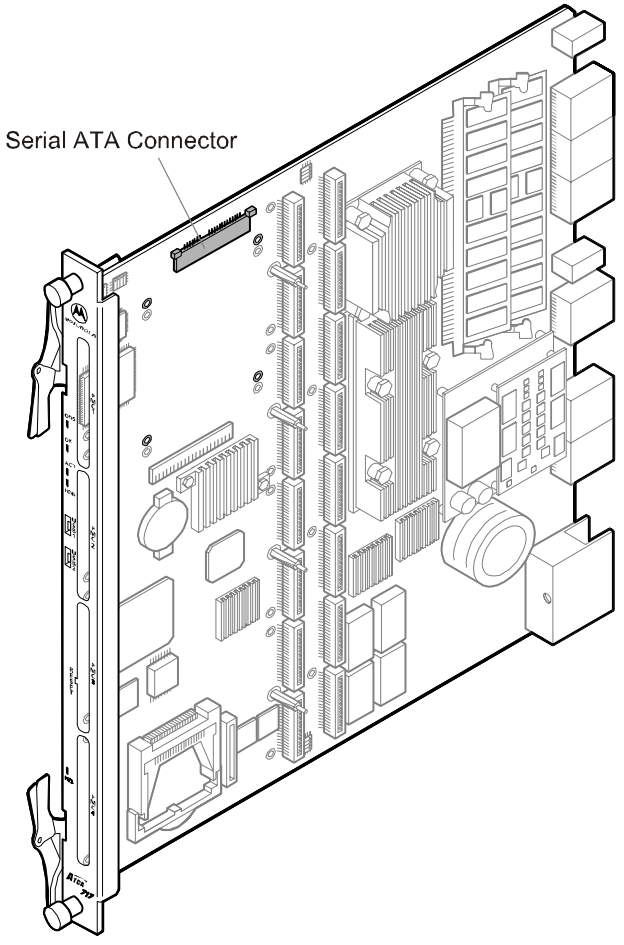


Figure 17: *Location of Serial ATA Connector*

The pinout of the SATA connector is given in the following figure.

1	GND
2	SATA0_TX+
3	SATA0_TX−
4	GND
5	SATA0_RX−
6	SATA0_RX+
7	GND

1	3.3V
2	3.3V
3	3.3V
4	GND
5	GND
6	GND
7	5V
8	5V
9	5V
10	GND
11	RSV
12	12V
13	12V
14	12V
15	12V

CMC Module Connector

The blade provides one CMC connector which allows to connect a CMC debug module to the blade. A CMC debug module is available as accessory kit for the blade. The CMC module uses the same mounting holes as PMC slot #4.

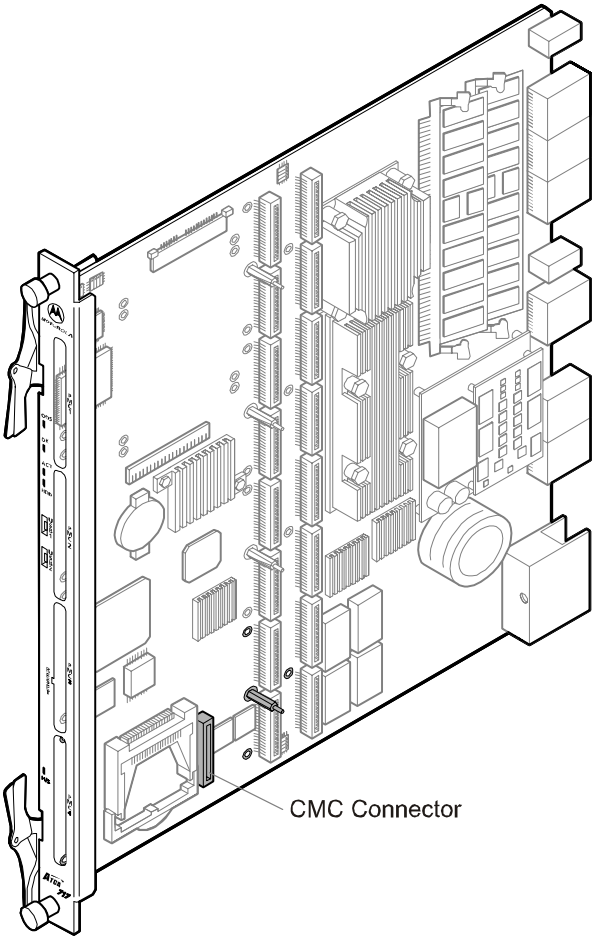
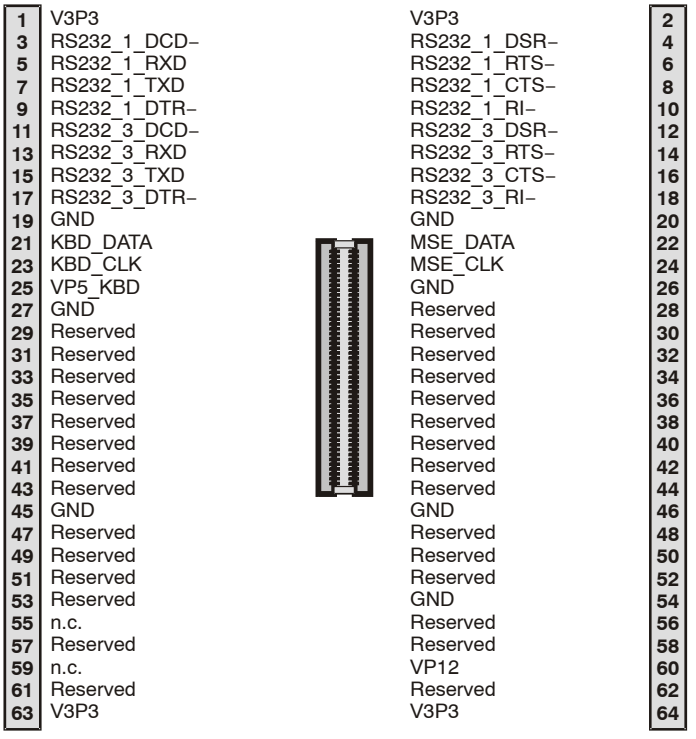


Figure 18: *Location of CMC Connector*

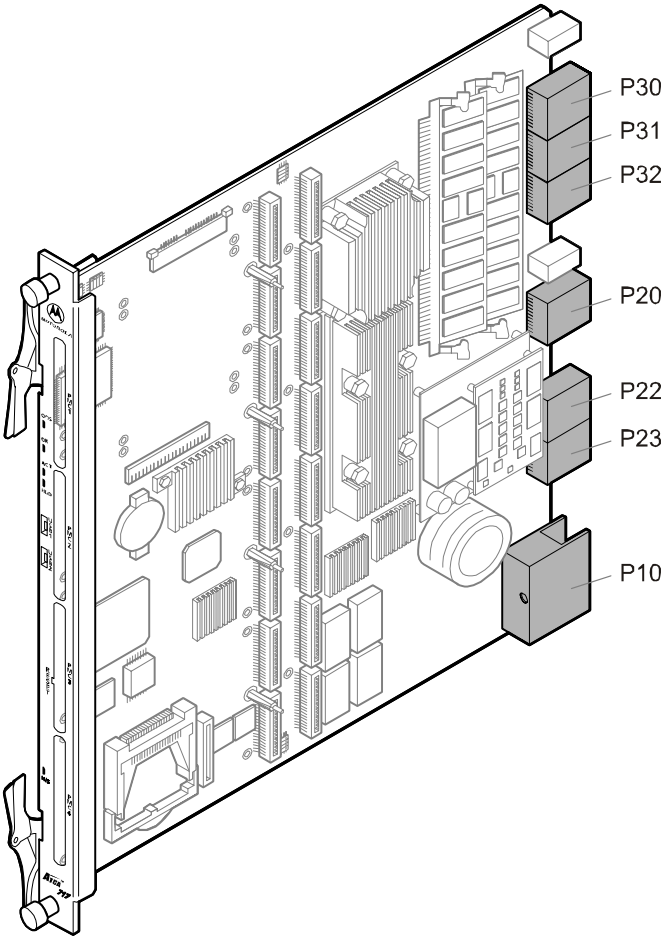
The pinout of the CMC connector is given in the following figure.



For further information about the CMC module refer to the *ACC/ATCA–CMC–MODULE Installation Guide.*

AdvancedTCA Backplane Connectors

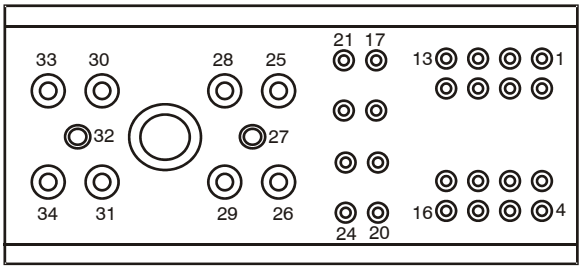
The AdvancedTCA backplane connectors reside in the three zones 1 to 3 as specified by the AdvancedTCA standard and are called P10, P20, P22, P23, P30, P31, and P32. The location of these connectors is shown in the following figure.



The pinouts of all these connectors are given in this section.

The connector residing in zone 1 is called P10 and carries the following signals:

- Power feed for the blade (ABP_VM48_x_CON and ABP_RTN_A_CON)
- Power enable (ABP_ENABLE_x)
- IPMB bus signals (APMB_P10_IPMB0_x_yyy)
- Geographic address signals (ABP_P10_HAx)
- Ground signals (ABP_P10_SHELF_GND and GND)
- Reserved signals



1	Reserved	18	n.c.
2	Reserved	19	n.c.
3	Reserved	20	n.c.
4	Reserved	21	n.c.
5	ABP_P10_HA0	22	n.c.
6	ABP_P10_HA1	23	n.c.
7	ABP_P10_HA2	24	n.c.
8	ABP_P10_HA3	25	ABP_P10_SHELF_GND
9	ABP_P10_HA4	26	GND
10	ABP_P10_HA5	27	ABP_ENABLE_B
11	ABP_P10_HA6	28	ABP_RTN_A_CON
12	ABP_P10_HA7	29	ABP_RTN_B_CON
13	ABP_P10_IPMB0_A_SCL	30	n.c.
14	ABP_P10_IPMB0_A_SDA	31	n.c.
15	ABP_P10_IPMB0_B_SCL	32	ABP_ENABLE_A
16	ABP_P10_IPMB0_B_SDA	33	ABP_VM48_A_CON
17	n.c.	34	ABP_VM48_B_CON

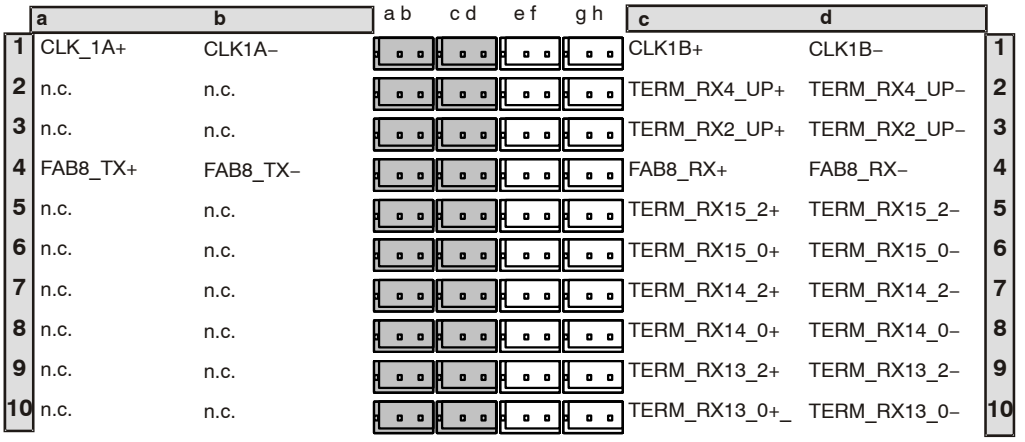
Figure 19: *P10 Backplane Connector Pinout*

Zone 2 contains the three connectors P20, P22 and P23. They carry the following types of signals:

- Telecom clock signals (CLKx_)
- Base interface signals (BASE_)
- Fabric channel interfaces (FAB_)

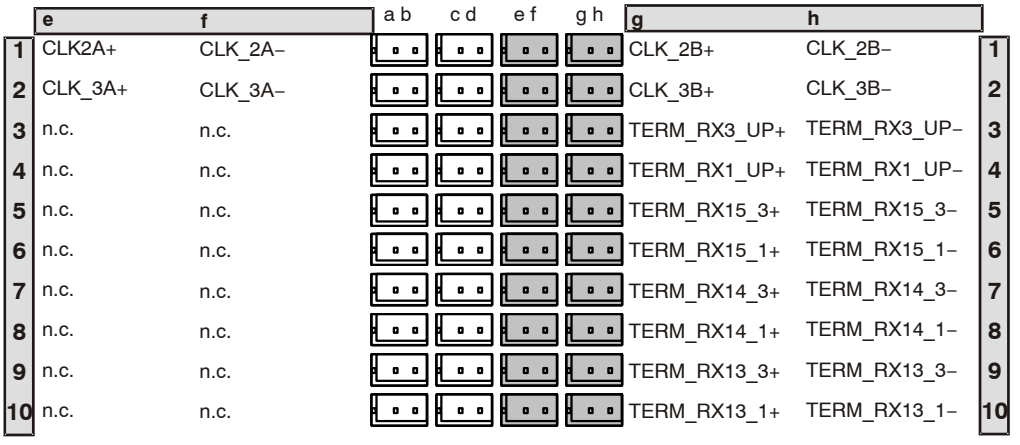
Some of the pins provided by P20, P21 and P23 are defined as optional in the AdvancedTCA specification and are unused on the blade. If the AdvancedTCA specification defines these signals as input signals, they are terminated on the blade and marked as "TERM_" in the following pinouts. In all other cases the pins are unconnected and consequently marked as "n.c.".

The pinouts of P20, P21 and P23 are as follows.



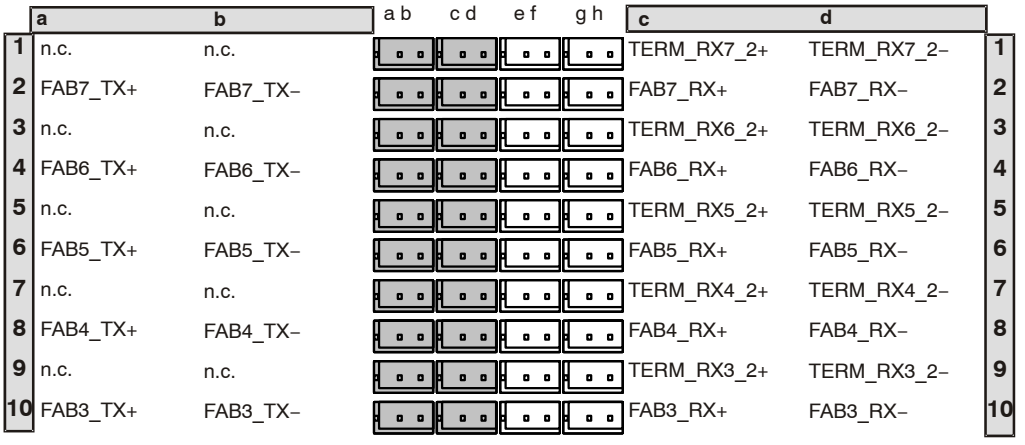
	a	b	ab cd ef gh	c	d	
1	CLK_1A+	CLK1A–		CLK1B+	CLK1B–	1
2	n.c.	n.c.		TERM_RX4_UP+	TERM_RX4_UP–	2
3	n.c.	n.c.		TERM_RX2_UP+	TERM_RX2_UP–	3
4	FAB8_TX+	FAB8_TX–		FAB8_RX+	FAB8_RX–	4
5	n.c.	n.c.		TERM_RX15_2+	TERM_RX15_2–	5
6	n.c.	n.c.		TERM_RX15_0+	TERM_RX15_0–	6
7	n.c.	n.c.		TERM_RX14_2+	TERM_RX14_2–	7
8	n.c.	n.c.		TERM_RX14_0+	TERM_RX14_0–	8
9	n.c.	n.c.		TERM_RX13_2+	TERM_RX13_2–	9
10	n.c.	n.c.		TERM_RX13_0+_	TERM_RX13_0–	10

Figure 20: *P20 Backplane Connector Pinout – Rows A to D*



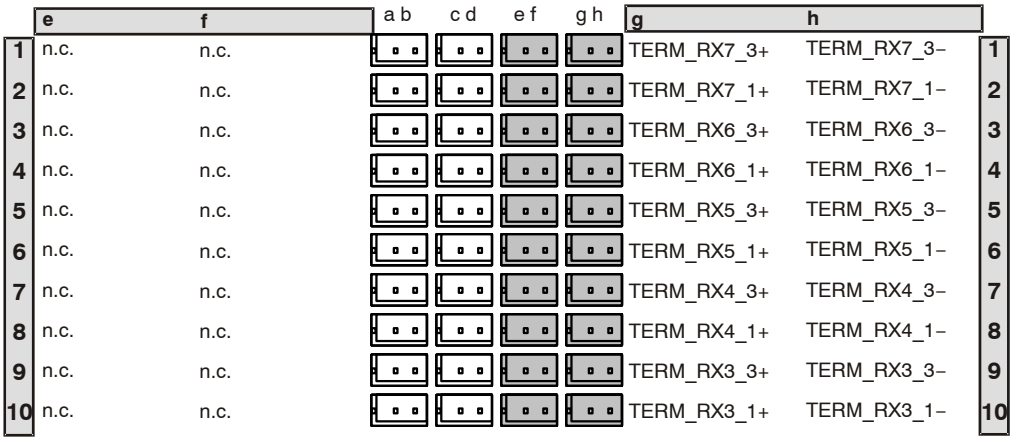
	e	f	ab cd ef gh	g	h	
1	CLK2A+	CLK_2A–		CLK_2B+	CLK_2B–	1
2	CLK_3A+	CLK_3A–		CLK_3B+	CLK_3B–	2
3	n.c.	n.c.		TERM_RX3_UP+	TERM_RX3_UP–	3
4	n.c.	n.c.		TERM_RX1_UP+	TERM_RX1_UP–	4
5	n.c.	n.c.		TERM_RX15_3+	TERM_RX15_3–	5
6	n.c.	n.c.		TERM_RX15_1+	TERM_RX15_1–	6
7	n.c.	n.c.		TERM_RX14_3+	TERM_RX14_3–	7
8	n.c.	n.c.		TERM_RX14_1+	TERM_RX14_1–	8
9	n.c.	n.c.		TERM_RX13_3+	TERM_RX13_3–	9
10	n.c.	n.c.		TERM_RX13_1+	TERM_RX13_1–	10

Figure 21: *P20 Backplane Connector Pinout – Rows E to H*



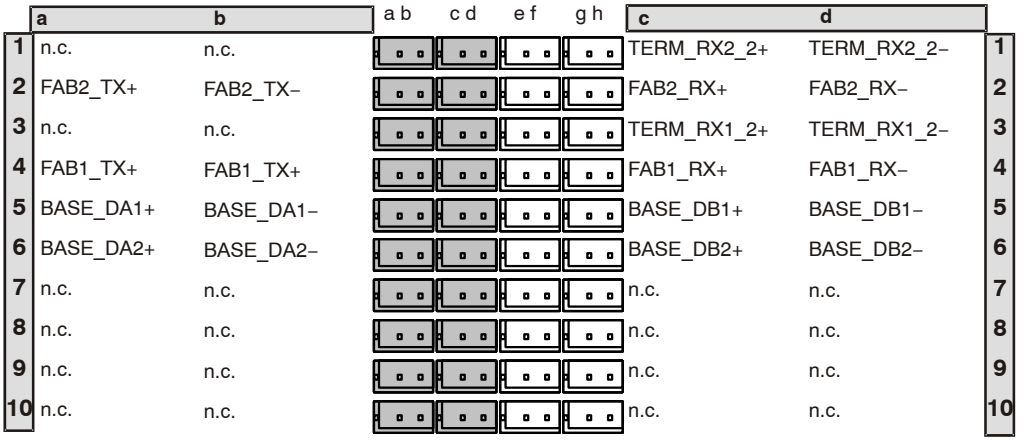
	a	b	ab cd ef gh	c	d	
1	n.c.	n.c.		TERM_RX7_2+	TERM_RX7_2–	1
2	FAB7_TX+	FAB7_TX–		FAB7_RX+	FAB7_RX–	2
3	n.c.	n.c.		TERM_RX6_2+	TERM_RX6_2–	3
4	FAB6_TX+	FAB6_TX–		FAB6_RX+	FAB6_RX–	4
5	n.c.	n.c.		TERM_RX5_2+	TERM_RX5_2–	5
6	FAB5_TX+	FAB5_TX–		FAB5_RX+	FAB5_RX–	6
7	n.c.	n.c.		TERM_RX4_2+	TERM_RX4_2–	7
8	FAB4_TX+	FAB4_TX–		FAB4_RX+	FAB4_RX–	8
9	n.c.	n.c.		TERM_RX3_2+	TERM_RX3_2–	9
10	FAB3_TX+	FAB3_TX–		FAB3_RX+	FAB3_RX–	10

Figure 22: *P22 Backplane Connector Pinout – Rows A to D*



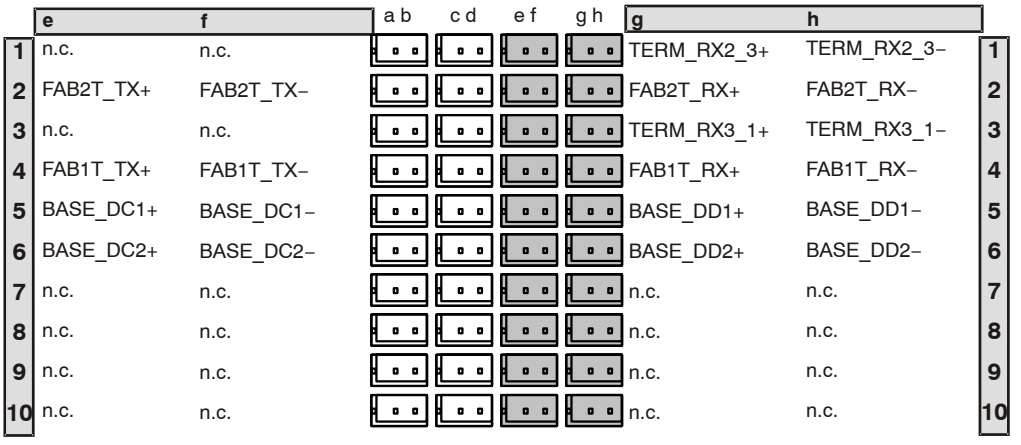
	e	f	g	h	
1	n.c.	n.c.	TERM_RX7_3+	TERM_RX7_3–	1
2	n.c.	n.c.	TERM_RX7_1+	TERM_RX7_1–	2
3	n.c.	n.c.	TERM_RX6_3+	TERM_RX6_3–	3
4	n.c.	n.c.	TERM_RX6_1+	TERM_RX6_1–	4
5	n.c.	n.c.	TERM_RX5_3+	TERM_RX5_3–	5
6	n.c.	n.c.	TERM_RX5_1+	TERM_RX5_1–	6
7	n.c.	n.c.	TERM_RX4_3+	TERM_RX4_3–	7
8	n.c.	n.c.	TERM_RX4_1+	TERM_RX4_1–	8
9	n.c.	n.c.	TERM_RX3_3+	TERM_RX3_3–	9
10	n.c.	n.c.	TERM_RX3_1+	TERM_RX3_1–	10

Figure 23: *P22 Backplane Connector Pinout – Rows E to H*



	a	b	c	d	
1	n.c.	n.c.	TERM_RX2_2+	TERM_RX2_2–	1
2	FAB2_TX+	FAB2_TX–	FAB2_RX+	FAB2_RX–	2
3	n.c.	n.c.	TERM_RX1_2+	TERM_RX1_2–	3
4	FAB1_TX+	FAB1_TX+	FAB1_RX+	FAB1_RX–	4
5	BASE_DA1+	BASE_DA1–	BASE_DB1+	BASE_DB1–	5
6	BASE_DA2+	BASE_DA2–	BASE_DB2+	BASE_DB2–	6
7	n.c.	n.c.	n.c.	n.c.	7
8	n.c.	n.c.	n.c.	n.c.	8
9	n.c.	n.c.	n.c.	n.c.	9
10	n.c.	n.c.	n.c.	n.c.	10

Figure 24: *P23 Backplane Connector Pinout – Rows A to D*

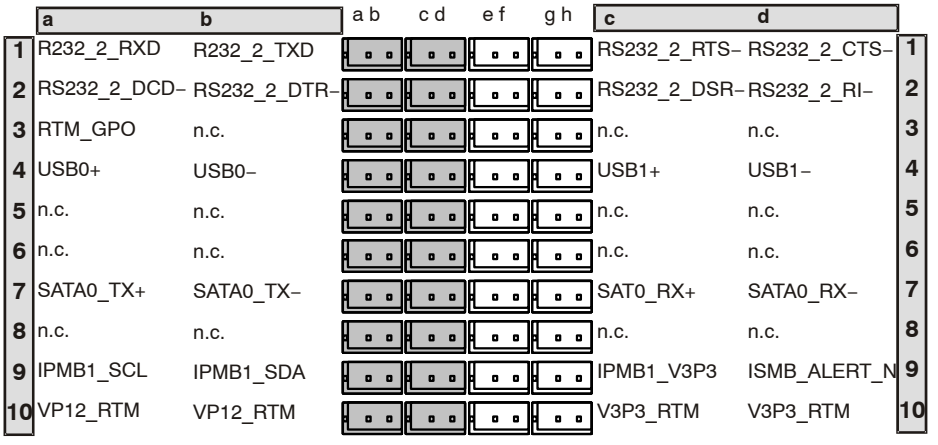


	e	f	g	h	
1	n.c.	n.c.	TERM_RX2_3+	TERM_RX2_3–	1
2	FAB2T_TX+	FAB2T_TX–	FAB2T_RX+	FAB2T_RX–	2
3	n.c.	n.c.	TERM_RX3_1+	TERM_RX3_1–	3
4	FAB1T_TX+	FAB1T_TX–	FAB1T_RX+	FAB1T_RX–	4
5	BASE_DC1+	BASE_DC1–	BASE_DD1+	BASE_DD1–	5
6	BASE_DC2+	BASE_DC2–	BASE_DD2+	BASE_DD2–	6
7	n.c.	n.c.	n.c.	n.c.	7
8	n.c.	n.c.	n.c.	n.c.	8
9	n.c.	n.c.	n.c.	n.c.	9
10	n.c.	n.c.	n.c.	n.c.	10

Figure 25: *P23 Backplane Connector Pinout – Rows E to H*

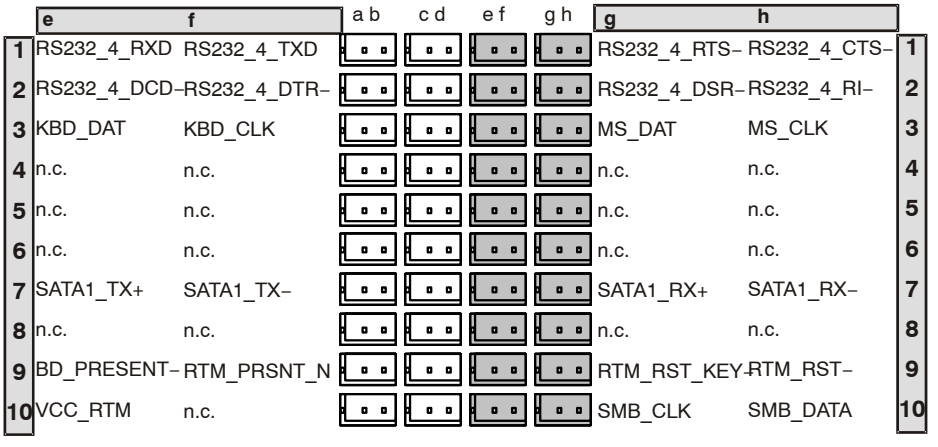
Zone 3 contains the three connectors P30 to P32. They are used to connect an RTM to the blade and carry the following signals

- Serial (RS232_x_yyyy)
- Serial ATA (SATAx_yyy)
- USB (USBxy)
- Keyboard/Mouse (KBD_xxx, MS_xxx)
- IPMI (IPMB1_xxx, ISMB_xxx))
- Power (VP12_RTM, V3P3_RTM)
- PMC user I/O (PMCx_IO_yy)
- General control signals (BD_PRESENTx, RTM_PRSNT_N, RTM_RST_KEY−, RTM_RST−)



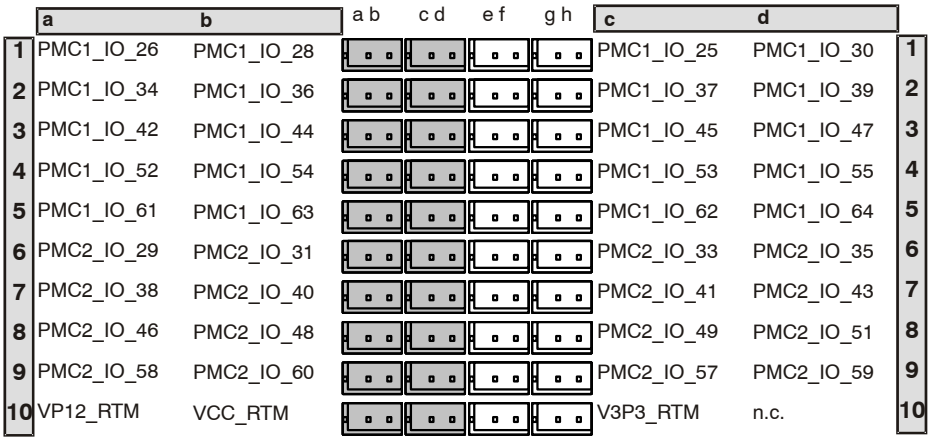
	a	b	a b	c d	e f	g h	c	d	
1	R232_2_RXD	R232_2_TXD					RS232_2_RTS−	RS232_2_CTS−	1
2	RS232_2_DCD−	RS232_2_DTR−					RS232_2_DSR−	RS232_2_RI−	2
3	RTM_GPO	n.c.					n.c.	n.c.	3
4	USB0+	USB0−					USB1+	USB1−	4
5	n.c.	n.c.					n.c.	n.c.	5
6	n.c.	n.c.					n.c.	n.c.	6
7	SATA0_TX+	SATA0_TX−					SAT0_RX+	SATA0_RX−	7
8	n.c.	n.c.					n.c.	n.c.	8
9	IPMB1_SCL	IPMB1_SDA					IPMB1_V3P3	ISMB_ALERT_N	9
10	VP12_RTM	VP12_RTM					V3P3_RTM	V3P3_RTM	10

Figure 26: *P30 Backplane Connector Pinout – Rows A to D*



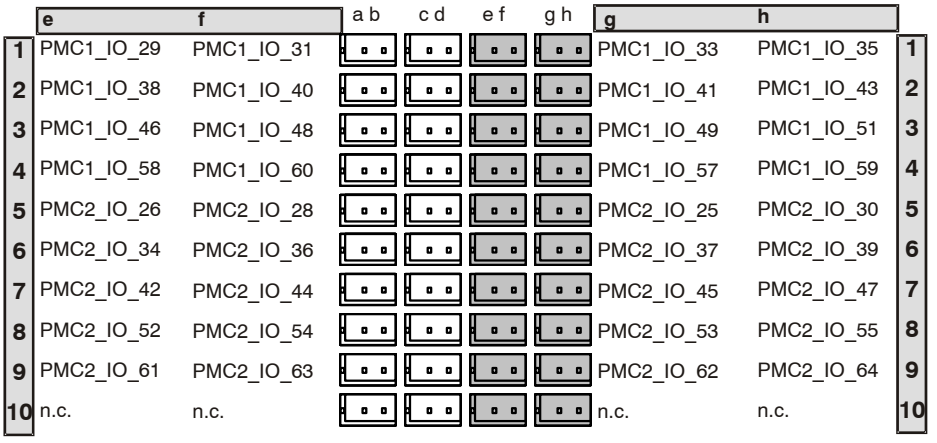
	e	f	a b	c d	e f	g h	g	h	
1	RS232_4_RXD	RS232_4_TXD					RS232_4_RTS−	RS232_4_CTS−	1
2	RS232_4_DCD−	RS232_4_DTR−					RS232_4_DSR−	RS232_4_RI−	2
3	KBD_DAT	KBD_CLK					MS_DAT	MS_CLK	3
4	n.c.	n.c.					n.c.	n.c.	4
5	n.c.	n.c.					n.c.	n.c.	5
6	n.c.	n.c.					n.c.	n.c.	6
7	SATA1_TX+	SATA1_TX−					SATA1_RX+	SATA1_RX−	7
8	n.c.	n.c.					n.c.	n.c.	8
9	BD_PRESENT−	RTM_PRSNT_N					RTM_RST_KEY−	RTM_RST−	9
10	VCC_RTM	n.c.					SMB_CLK	SMB_DATA	10

Figure 27: *P30 Backplane Connector Pinout – Rows E to H*



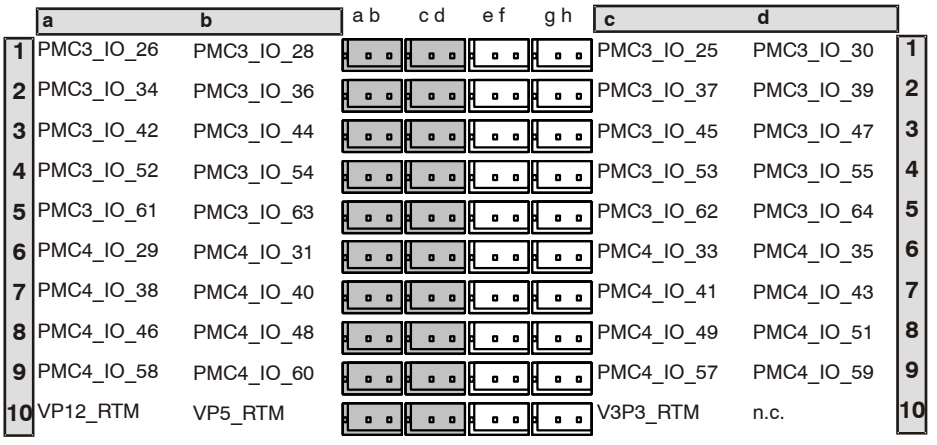
	a	b	c	d	
1	PMC1_IO_26	PMC1_IO_28	PMC1_IO_25	PMC1_IO_30	1
2	PMC1_IO_34	PMC1_IO_36	PMC1_IO_37	PMC1_IO_39	2
3	PMC1_IO_42	PMC1_IO_44	PMC1_IO_45	PMC1_IO_47	3
4	PMC1_IO_52	PMC1_IO_54	PMC1_IO_53	PMC1_IO_55	4
5	PMC1_IO_61	PMC1_IO_63	PMC1_IO_62	PMC1_IO_64	5
6	PMC2_IO_29	PMC2_IO_31	PMC2_IO_33	PMC2_IO_35	6
7	PMC2_IO_38	PMC2_IO_40	PMC2_IO_41	PMC2_IO_43	7
8	PMC2_IO_46	PMC2_IO_48	PMC2_IO_49	PMC2_IO_51	8
9	PMC2_IO_58	PMC2_IO_60	PMC2_IO_57	PMC2_IO_59	9
10	VP12_RTM	VCC_RTM	V3P3_RTM	n.c.	10

Figure 28: *P31 Backplane Connector Pinout – Rows A to D*



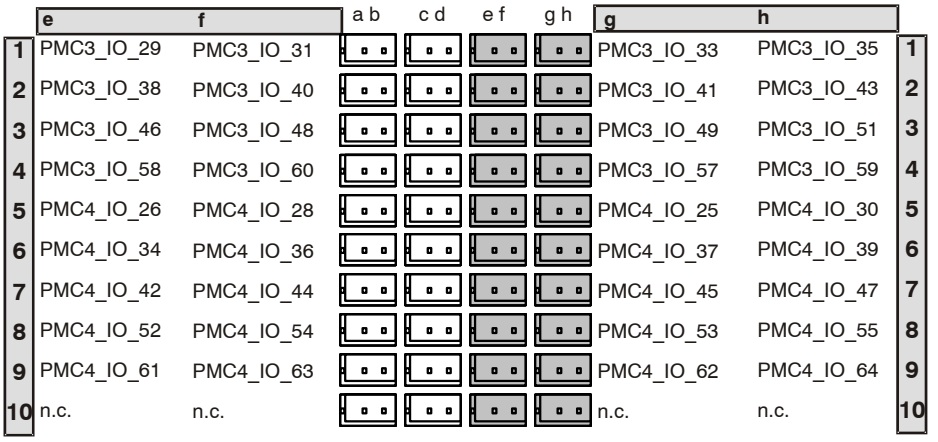
	e	f	g	h	
1	PMC1_IO_29	PMC1_IO_31	PMC1_IO_33	PMC1_IO_35	1
2	PMC1_IO_38	PMC1_IO_40	PMC1_IO_41	PMC1_IO_43	2
3	PMC1_IO_46	PMC1_IO_48	PMC1_IO_49	PMC1_IO_51	3
4	PMC1_IO_58	PMC1_IO_60	PMC1_IO_57	PMC1_IO_59	4
5	PMC2_IO_26	PMC2_IO_28	PMC2_IO_25	PMC2_IO_30	5
6	PMC2_IO_34	PMC2_IO_36	PMC2_IO_37	PMC2_IO_39	6
7	PMC2_IO_42	PMC2_IO_44	PMC2_IO_45	PMC2_IO_47	7
8	PMC2_IO_52	PMC2_IO_54	PMC2_IO_53	PMC2_IO_55	8
9	PMC2_IO_61	PMC2_IO_63	PMC2_IO_62	PMC2_IO_64	9
10	n.c.	n.c.	n.c.	n.c.	10

Figure 29: *P31 Backplane Connector Pinout – Rows E to H*



	a	b	c	d	
1	PMC3_IO_26	PMC3_IO_28	PMC3_IO_25	PMC3_IO_30	1
2	PMC3_IO_34	PMC3_IO_36	PMC3_IO_37	PMC3_IO_39	2
3	PMC3_IO_42	PMC3_IO_44	PMC3_IO_45	PMC3_IO_47	3
4	PMC3_IO_52	PMC3_IO_54	PMC3_IO_53	PMC3_IO_55	4
5	PMC3_IO_61	PMC3_IO_63	PMC3_IO_62	PMC3_IO_64	5
6	PMC4_IO_29	PMC4_IO_31	PMC4_IO_33	PMC4_IO_35	6
7	PMC4_IO_38	PMC4_IO_40	PMC4_IO_41	PMC4_IO_43	7
8	PMC4_IO_46	PMC4_IO_48	PMC4_IO_49	PMC4_IO_51	8
9	PMC4_IO_58	PMC4_IO_60	PMC4_IO_57	PMC4_IO_59	9
10	VP12_RTM	VP5_RTM	V3P3_RTM	n.c.	10

Figure 30: *P32 Backplane Connector Pinout – Rows A to D*



	e	f	a b	c d	e f	g h	g	h	
1	PMC3_IO_29	PMC3_IO_31					PMC3_IO_33	PMC3_IO_35	1
2	PMC3_IO_38	PMC3_IO_40					PMC3_IO_41	PMC3_IO_43	2
3	PMC3_IO_46	PMC3_IO_48					PMC3_IO_49	PMC3_IO_51	3
4	PMC3_IO_58	PMC3_IO_60					PMC3_IO_57	PMC3_IO_59	4
5	PMC4_IO_26	PMC4_IO_28					PMC4_IO_25	PMC4_IO_30	5
6	PMC4_IO_34	PMC4_IO_36					PMC4_IO_37	PMC4_IO_39	6
7	PMC4_IO_42	PMC4_IO_44					PMC4_IO_45	PMC4_IO_47	7
8	PMC4_IO_52	PMC4_IO_54					PMC4_IO_53	PMC4_IO_55	8
9	PMC4_IO_61	PMC4_IO_63					PMC4_IO_62	PMC4_IO_64	9
10	n.c.	n.c.					n.c.	n.c.	10

Figure 31: *P32 Backplane Connector Pinout – Rows E to H*

4

BIOS

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Introduction

BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the blade. It is used for hardware configuration. Before loading the operating system, BIOS performs basic hardware tests and prepares the blade for the initial boot–up procedure.

During blade production, identical BIOS images are programmed into the blade's boot and user flash. By default the blade boots from the boot flash. It is possible to select between boot and user flash as device to boot from. This is done via a OEM IPMI command. For further details refer to the *PENT/ATCA–715/717/7105/7107: Control via IPMI Programmer's Guide* which can be downloaded from the Motorola literature catalog. The presence of two redundant flash devices also allows for updating the BIOS image without affecting running processes.

The BIOS used on the blade is based on the Phoenix 4.0 Release 6.0 BIOS with several Motorola extensions integrated. Its main functions are:

- Hardware set–up utility for setting configuration data
- Multiboot for a flexible boot order
- Serial console redirection for remote blade configuration
- Software upgrade utility

Note: The BIOS contains on–line documentation which provides detailed description of all BIOS functions. Therefore the description in this manual is restricted to the main BIOS functions.

The BIOS set–up program is required to configure the hardware of the blade. This configuration is necessary for operating the blade and connected peripherals. It is stored in the battery backed–up CMOS memory as well as in the blade's boot flash.

Whenever you are not sure about configuration settings, restore the default values. They are provided in case a value has been changed and you wish to reset settings. To restore the default values, press <F9> in setup.

Note:

- **Loading the BIOS default values will affect all set–up items and will reset options previously altered.**
- **If you set the default values, the displayed default values are not yet stored to be effective for the next boot. They are just loaded to be displayed. However, they become effective if the BIOS setup is exited after changes have been saved.**

The BIOS complies to the following specifications:

- Plug and Play BIOS Specification 1.0A
- PCI BIOS Specification 2.1
- SMBIOS Specification 2.3
- BIOS Boot Specification 1.01
- PXE 2.0

Serial Console Redirection

The firmware of the blade provides a serial console redirection feature. This allows remote blade configuration by connecting a terminal to the blade via a serial communication link.

The terminal can be connected to display VGA text information. Terminal keyboard input is redirected and treated as a normal PC keyboard input. The serial console redirection feature can be configured via setup utility.

Note: If serial console redirection is enabled the terminal represents an option and is not necessarily required for boot-up procedure.

Requirements

For serial console redirection, the following is required:

- Terminal which supports a VT100 or ANSI mode
- NULL-modem cable

Terminal emulation programs such as TeraTermPro can be used. In order to use TeraTermPro via the function keys, the keyboard configuration file of TeraTermPro has to be modified as follows:

Table 8: *Key Codes for Terminal Emulation Program*

Function Key	Key Code
PF1	59
PF2	60

Default Configuration

By default, the blade can be accessed via the serial interface COM1. This interface is, by default, accessible via an installed RTM through an RJ-45 connector. If no RTM is present or you wish to access COM1 from the blade's face plate, COM1 can alternatively be made accessible at an installed CMC module. Whether COM1 is available via RTM or CMC module depends on the setting of the on-board switch SW3-4 which enables/disables COM port swapping. The following table provides details.

Setting of SW3-4	COM1 is accessible via:
OFF (default)	RTM (upper serial connector)
ON	CMC module (upper serial connector)

Note:

- **The COM port routing described above is only applicable to BIOS versions ≥ 2.0.0. Earlier BIOS versions used a different routing. For details refer to the *PENT/ATCA-715/717/7105/7107 BIOS Information Sheet* which can be downloaded from the Motorola literature catalog web site.**
- **COM port swapping can also be enabled via an IPMI System Boot Options command. COM port swapping is enabled if either the on-board switch 3-4, the IPMI System Boot Options command or both enable it.**

A NULL-Modem cable is available as accessory kit for the blade. It converts the RJ-45 connector to a standard DSUB connector which can be connected to a remote terminal. The following communication parameters are used by default:

- Baud rate: 9600
- No handshake
- PC ANSI
- 8 data bits
- No parity
- 1 stop bit

All configuration parameters listed above can be modified via the BIOS.

Connecting to the Blade

In order to connect to the blade using the serial console redirect feature, proceed as follows:.

Procedure

1. Configure terminal to communicate using the same parameters as in BIOS setup
2. Connect terminal to NULL-modem cable
3. Connect NULL-modem cable to COM port you have selected in BIOS setup
4. Start up blade

BIOS Crisis Recovery Mode

Immediately after a reset or power–up a routine in the boot flash boot block is invoked which checks whether a valid BIOS image is available. If no valid image is found and consequently the blade is unable to boot, the blade enters into BIOS crisis recovery mode. In this mode a routine tries to load a BIOS crisis recovery image from a disk drive connected to the blade' s USB interface. The BIOS crisis recovery image is basically a mini DOS with minimum functionality which replaces the corrupted image.

A valid BIOS crisis recovery image can be downloaded from the former Force Computers SMART server or the Motorola website as part of the BIOS upgrade kit which which is available for this blade. The image is accompanied by readme files which describe how to create the BIOS upgrade/recovery disk and how to to replace a corrupted BIOS with the BIOS crisis recovery image.

If the blade has enterred BIOS crisis recovery mode,the face plate LED "HDD" is lit ed. After the BIOS recovery image has been successfully flashed, the LED is lit green.

Note: Flashing the BIOS crisis recovery image may take up to two minutes. In order to avoid blade damage, it is absolutely important not to interrupt the flashing process. Therefore wait until the LED is lit green again, which indicates a successful flashing.

Changing Configuration Settings

When the system is turned on or rebooted, the presence and functionality of the system components is tested by POST (Power–On Self–Test).

Press <F2> when requested. The main menu appears. It looks similar to the menu shown in the following figure. Note that the layout may slightly vary with new BIOS versions.

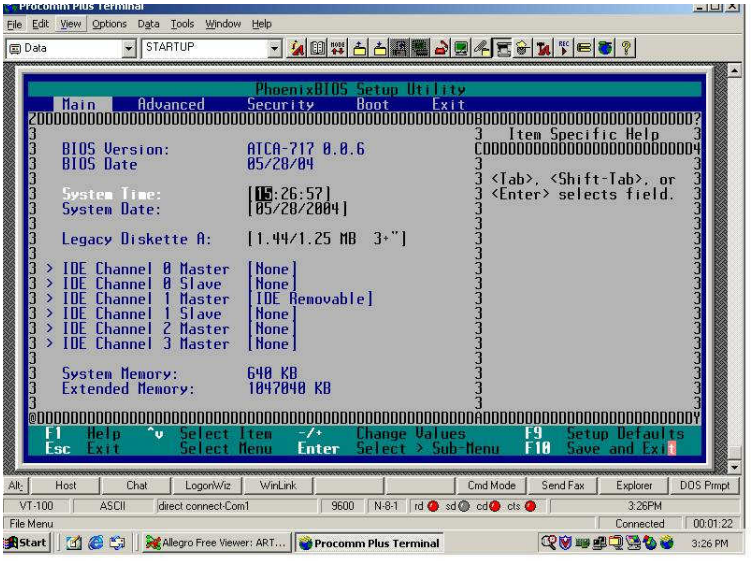

PhoenixBIOS Setup Utility
Main Advanced Security Boot Exit
BIOS Version: ATCA-717 0.0.6
BIOS Date 05/28/04
System Time: [15:26:57]
System Date: [05/28/2004]
Legacy Diskette A: [1.44/1.25 MB 3½"]
> IDE Channel 0 Master [None]
> IDE Channel 0 Slave [None]
> IDE Channel 1 Master [IDE Removable]
> IDE Channel 1 Slave [None]
> IDE Channel 2 Master [None]
> IDE Channel 3 Master [None]
System Memory: 640 KB
Extended Memory: 1047040 KB
Item Specific Help
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
Esc Exit ↔ Select Menu Enter Select > Sub-Menu F10 Save and Exit

Figure 32: *Main Menu*

Note:

- **Make sure that BIOS is properly configured prior to installing the operating system and its drivers.**
- **If you save changes in setup, the next time the blade boots BIOS will configure the system according to the setup selections stored. If those values cause the system boot to fail, reboot and enter setup to get the default values or to change the selections that caused the failure. If the boot fails or is interrupted three times in a row, the default values are then loaded automatically.**

In order to navigate in setup, use the arrow keys on the keyblade to highlight items on the menu. All other navigation possibilities are shown at the bottom of the menu.

Additionally, an item–specific help is displayed on the right side of the menu window.

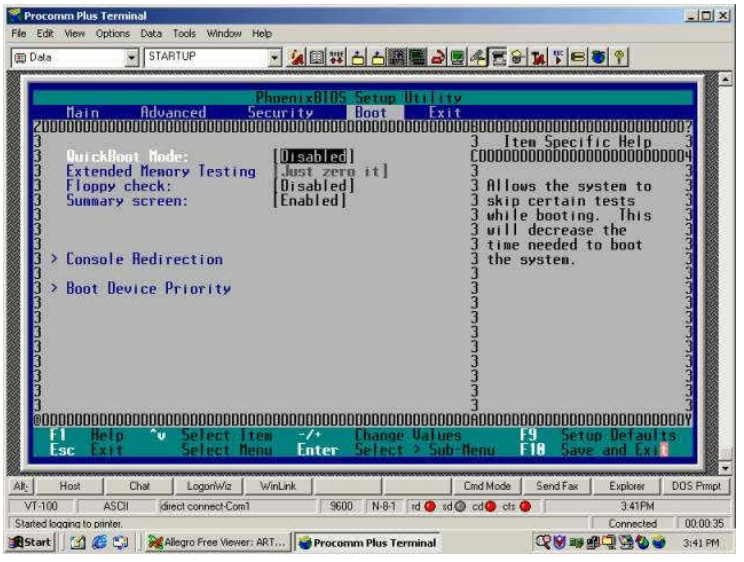
Selecting The Boot Device

There are two possibilities to determine the device from which BIOS attempts to boot:

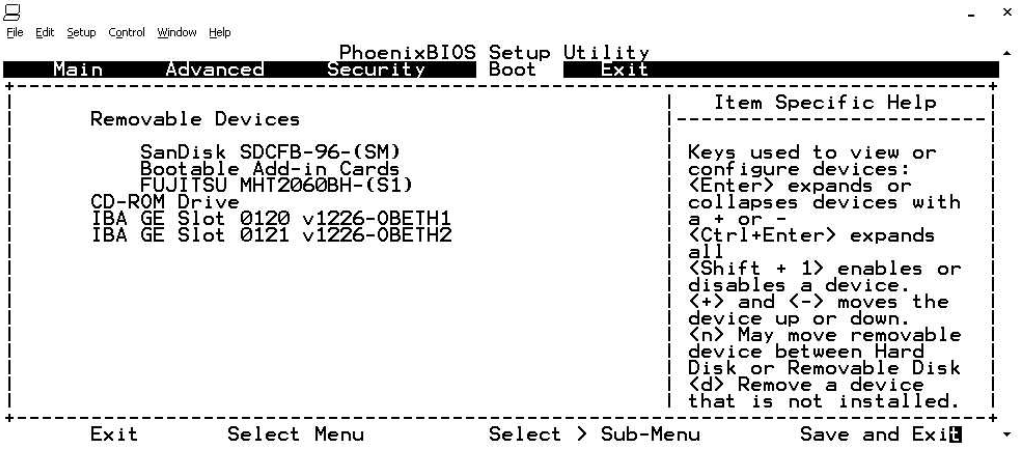
- Via setup to select a permanent order of boot devices
- Via boot selection menu to select any device for the next boot-up procedure only

Via Setup

1. In the menu line, select [Boot]
   A menu similar to the one shown in the following figure appears. Note that the layout may vary slightly with new BIOS versions.


Procomm Plus Terminal
File Edit View Options Data Tools Window Help
Data
STARTUP
PhoenixBIOS Setup Utility
Main Advanced Security Boot Exit
QuickBoot Mode: [Disabled]
Extended Memory Testing [Just zero it]
Floppy check: [Disabled]
Summary screen: [Enabled]
> Console Redirection
> Boot Device Priority
Item Specific Help
Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
F1 Help ^v Select Item -/+ Change Values F9 Setup Defaults
Esc Exit Select Menu Enter Select > Sub-Menu F10 Save and Exit
Host Chat LogonWiz WinLink Cmd Mode Send Fax Explorer DOS Prmpt
VT-100 ASCII direct connect-Com1 9600 N-8-1 rd sd cd cts 3:41PM
Started logging to printer. Connected 00:00:35
Start Allegro Free Viewer: ART... Procomm Plus Terminal 3:41 PM

2. Select [Boot Device Priority]
   A menu similar to the one shown in the following figure appears. Note that the layout may vary slightly with new BIOS versions.


File Edit Setup Control Window Help
PhoenixBIOS Setup Utility
Main Advanced Security Boot Exit
Removable Devices
SanDisk SDCFB-96-(SM)
Bootable Add-in Cards
FUJITSU MHT2060BH-(S1)
CD-ROM Drive
IBA GE Slot 0120 v1226-0BETH1
IBA GE Slot 0121 v1226-0BETH2
Item Specific Help
Keys used to view or configure devices:
<Enter> expands or collapses devices with a + or -
<Ctrl+Enter> expands all
<Shift + 1> enables or disables a device.
<+> and <-> moves the device up or down.
<n> May move removable device between Hard Disk or Removable Disk
<d> Remove a device that is not installed.
Exit
Select Menu
Select > Sub-Menu
Save and Exit

3. Select the order of the devices from which BIOS attempts to boot the operating system

If BIOS is not successful at booting from one device, it tries to boot from the next device on the list.

If there is more than one device of the same type, e.g. several hard disks, the displayed entry represents the first of these devices as specified in the boot configuration via setup.

The same options determine the order in which POST installs the devices and the operating system assigns device letters. BIOS supports up to two floppy devices to which the operating system may assign, e.g. drive letters A: and B:. The drives C:, D:, E: etc. are reserved for hard-disk drives.

Note: There is not always an exact correspondence between the order specified in setup and the letters assigned by the operating system. Many devices, such as legacy option ROMs, support more than one device that can be assigned to several letters. If the CD-ROM drive should have a letter coming before the one assigned to the hard drive, move it in front of the hard drive. The group of bootable add-in cards refers to devices with non-multiboot-compliant BIOS option ROM from which you can boot the operating system.

Via Boot Selection Menu

To enter the boot menu, press <ESC> during POST. The menu that appears looks similar to the one shown in the following figure. Note that the layout may vary slightly with new BIOS versions.

Figure 33: *Boot Menu*

Continue with one of the following options:

a) Override existing boot sequence by selecting another boot device from the boot order list or

b) Select [Enter Setup] to enter setup utility or

c) Press <Esc> to return to POST screen and continue with previous boot sequence

---

Note: If the selected device does not load the operating system, BIOS reverts to the previous boot sequence.

Restoring BIOS Default Settings

The blade provides an on-board configuration switch that allows to clear the blade's CMOS and thus to restore the BIOS default settings. In order to restore the BIOS default settings using this switch, you have to proceed as follows.

Procedure

1. Remove the blade from the system
   See section "Installation into Powered Shelves" on page 54 for the exact procedure
2. Set the on-board switch SW2-3 to ON
   See section "Switch Settings" on page 42 for the exact location of SW2-3
3. Install and power up the blade
   See section "Installation into Powered Shelves" on page 54 for the exact procedure.
   Note that the blade will not boot, because the "Clear CMOS RAM" switch SW2-3 is set to ON.
4. Remove the blade from the system again
   See section "Installation into Powered Shelves" on page 54 for the exact procedure
5. Set switch SW2-3 to OFF
   Now the BIOS default settings are restored.

Updating BIOS

For the blade a BIOS upgrade kit is offered. It is available via the former Force Computers S.M.A.R.T. web site or the Motorola web site.

Note: When upgrading the BIOS, all BIOS settings are reset to their default state.

BIOS Messages

If your system fails after you made changes in the setup menus, you may be able to correct the problem by entering setup and restoring the original values.

Message	Explanation	Corrective Action
`nnnn Cache SRAM Passed`	nnnn is amount of system cache in KBytes successfully tested	None
`CD-ROM Drive Identified`	Autotyping identified CD-ROM Drive	None
`Diskette drive A errorDiskette drive B error`	Drive A: or B: fails the BIOS POST disk tests. Drive is selected via setup but either not present or defect.	Check that drive is defined with proper disk type in setup, that disk drive is attached correctly and that controller is enabled.
`Entering SETUP ...`	Starting setup program	None
`Extended RAM Failed at offset: nnnn`	Extended memory not working or not configured properly at offset nnnn	Check if memory modules are installed correctly. Otherwise contact your local sales representative or FAE for further support.
`nnnn Extended RAM Passed`	nnnn is amount of RAM in MBytes successfully tested.	None
`Failing Bits: nnnn`	nnnn is a map of the bits at the RAM address (in system, extended or shadow memory) which failed the memory test. Each 1 (one) in the map indicates a failed bit.	Check if memory modules are installed correctly. Otherwise contact your local sales representative or FAE for further support.

`Fixed Disk 0 Failure`
`Fixed Disk 1 Failure`
`Fixed Disk Controller Failure`
	Fixed disk not working or not configured properly	Check if fixed disk is attached properly. Run setup to be sure the fixed-disk type is correctly identified.

`Fixed Disk 0...3 Identified`	Autotyping identified specified fixed disk	None
`Incorrect Drive A type - run SETUP` `Incorrect Drive B type - run SETUP`	Type of floppy drive not correctly identified in setup	Check for correct floppy drive in setup.
`Keyblade controller error`	Keyblade controller failed test	Replace keyblade

Message	Explanation	Corrective Action
`Keyblade error`	Keyblade not working	Check for correct keyblade connection.
`Keyblade error nnn`	BIOS discovered a stuck key and displays scan code nn for stuck key	Replace keyblade, check for stuck keys
`Operating system not found`	Operating system cannot be located on either drive A: or drive C:.	Enter setup and check if fixed disk and drive A: are properly identified.
`Parity Check 1 nnnn`	Parity error found in system bus. BIOS attempts to locate address nnnn and display it on screen. If it cannot locate the address, it displays ????.	Check for correct memory module types.
`Parity Check 2 nnnn`	Parity error found in system bus. BIOS attempts to locate address nnnn and display it on the screen. If it cannot locate the address, it displays ????.	Check for correct memory module types.
`Press <F1> to resume, <F2> to setup`	Displayed after any recoverable error message	Press <F1> to start boot process or <F2> to enter setup and change any settings.
`Previous boot incomplete - Default configuration used`	Previous POST did not complete successfully. POST loads default values and offers to run setup. If failure was caused by incorrect values and they are not corrected, the next boot will likely fail.	Run setup to restore original configuration. This error is cleared the next time the system is booted.
`Real time clock error`	Real-time clock fails BIOS test	May require blade repair
`Resource allocation conflict on motherblade - Run Configuration Utility`	Possible interrupt or interface resource conflict.	Run ISA or EISA Configuration Utility to resolve resource conflict.
`Shadow RAM Failed at offset: nnnn`	Shadow RAM failed at offset nnnn of the 64k block at which error was detected.	Contact your local sales representative or FAE for further support.
`nnnn Shadow RAM Passed`	nnnn is amount of shadow RAM in KBytes successfully tested	None

Message	Explanation	Corrective Action
`System battery is dead - Replace and run SETUP`	The NVRAM (CMOS) clock battery indicator shows the battery is dead.	Replace battery and run setup to reconfigure system.
`System BIOS shadowed`	System BIOS copied to shadow RAM	None
`System cache error - Cache disabled`	RAM cache failed BIOS test. BIOS disabled cache	Contact your local sales representative or FAE for further support.
`System CMOS checksum bad - run SETUP`	System NVRAM (CMOS) has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in NVRAM (CMOS).	Run setup and reconfigure system either by getting default values and/or making your own selections.
`System RAM Failed at offset: nnnn`	System RAM failed at offset nnnn in the 64k block at which the error was detected.	Check for correct memory modules. Otherwise contact your local sales representative or FAE for further support.
`nnnn System RAM Passed`	nnnn is amount of system RAM in KBytes successfully tested	None
`System timer error`	Timer test failed	Requires repair of system blade
`UMB upper limit segment address: nnnn`	Address nnnn of the upper limit of upper memory blocks indicates released segments of BIOS which may be reclaimed by a virtual memory manager.	None
`Video BIOS shadowed`	Video BIOS successfully copied to shadow RAM	None
`Invalid System Configuration Data - run configuration utility`	-	Enter setup and use advanced configuration option to reset configuration data (due to corrupted ESCD data).

BIOS Post Codes

The following table lists BIOS post codes applicable to the used Phoenix 4.0 Release 6.0 BIOS. The BIOS POST codes are stored in the blade's Port 80 register and can also be obtained by reading an on-board IPMI sensor. For details refer to the *PENT/ATCA−715/717/7105/7107*: Control via IPMI Programmer's Guide which can be downloaded from the Motorola literature catalog.

Table 9: *Standard BIOS Post Codes*

Post Code	Description
02	Verify real mode
03	Disable non-maskable interrupt (NMI)
04	Get CPU type
06	Initialize system hardware
07	Disable shadow and execute code from the ROM
08	Initialize chipset with initial POST values
09	Set IN POST flag
0A	Initialize CPU registers
0B	Enable CPU cache
0C	Initialize caches to initial POST values
0E	Initialize I/O component
0F	Initialize the local bus IDE
10	initialize power management
11	Load alternate registers with initial POST values
12	Restore CPU control word during warm boot
13	Initialize PCI bus mastering devices
14	Initialize keyboard controller
16	BIOS ROM checksum
17	Initialize cache before memory autosize
18	8254 programmable interrupt timer initialization
1A	8237 DMA controller initialization
1C	Reset programmable interrupt controller
20	Test DRAM refresh
22	Test 8742 keyboard controller

Post Code	Description
24	Set ES segment register to 4GB
26	Enable gate A20 line
28	Autosize DRAM
29	Initialize POST memory manager
2A	Clear 512KB base RAM
2C	RAM failure on address line xxxx
2E	RAM failure on data bits xxxx of low byte of memory bus
2F	Enable cache before system BIOS shadow
30	RAM failure on data bits xxxx of high byte of memory bus
32	Test CPU bus clock frequency
33	Initialize Phoenix Dispatch Manager
36	Warm start shut down
38	Shadow system BIOS ROM
3A	Autosize cache
3C	Advanced configuration of chipset registers
3D	Load alternate registers with CMOS values
41	Initialize extended memory for RomPilot
42	Initialize interrupt vectors
45	POST device initialization
46	Check ROM copyright notice
47	Initialize I20 support
48	Check video configuration against CMOS
49	Initialize PCI bus and devices
4A	Initialize all video adapters in system
4B	QuietBoot start (optional)
4C	Shadow video BIOS ROM
4E	Display BIOS copyright notice
4F	Initialize MultiBoot
50	Display CPU type and speed
51	Initialize EISA board

Post Code	Description
52	Test keyboard
54	Set key click if enabled
55	Enable USB devices
58	Test for unexpected interrupts
59	Initialize POST display service
5A	Display prompt ″Press F2 to enter SETUP″
5B	Disable CPU cache
5C	Test RAM between 512KB and 640KB
60	Test extended memory
62	Test extended memory address lines
64	Jump to UserPatch1
66	Configure advanced cache registers
67	Initialize Multi Processor APIC
68	Enable external and CPU caches
69	Setup system management mode (SMM) area
6A	Display external L2 cache size
6B	Load custom defaults (optional)
6C	Display shadow area message
6E	Display possible high address for UMB recovery
70	Display error messages
72	Check for configuration errors
76	Check for keyboard errors
7C	Set up hardware interrupt vectors
7D	Initialize Intelligent System Monitoring
7E	Initialize coprocessor if present
80	Disable onboard super I/O ports and IRQ's
81	Late POST device initialization
82	Detect and install external RS232 ports
83	Configure non-MCD IDE controllers
84	Detect and install external parallel ports

Post Code	Description
85	Initialize PC compatible PnP ISA devices
86	Reinitialize onboard I/O ports
87	Configure motherboard configurable devices (optional)
88	Initialize BIOS data area
89	Enable non–maskable interrupts (NMI's)
8A	Initialize extended BIOS data area
8B	Test and initialize PS/2 mouse
8C	Initialize floppy controller
8F	Determine number of ATA drives (optional)
90	Initialize hard disk controllers
91	Initialize local bus hard disk controllers
92	Jump to UserPatch2
93	Build MPTABLE for multi processor boards
95	Install CD ROM for boot
96	Clear huge ES segment register
97	Fixup multi processor table
98	Search for option ROM's
99	Check for SMART drive (optional)
9A	Shadow option ROM's
9C	Set up power management
9D	Initialize security engine (optional)
9E	Enable hardware interrupts
9F	Determine number of ATA and SCSI drives
A0	Set time of day
A2	Check key lock
A4	Initialize typematic rate
A8	Erase F2 prompt
AA	Scan for F2 key stroke
AC	Enter setup
AE	Clear boot flag

Post Code	Description
B0	Check for errors
B1	Inform RomPilot about the end of POST
B2	POST done – prepare to boot operating system
B4	One short beep
B5	Terminate QuietBoot (optional)
B6	Check password
B7	Initialize ACPI BIOS
B9	Prepare boot
BA	Initialize DMI parameters
BB	Initialize PnP option ROM's
BC	Clear parity checkers
BD	Display multiboot menu
BE	Clear screen
BF	Check virus and backup reminders
C0	Try to boot with interrupt 19
C1	Initialize POST Error Manager (PEM)
C2	Initialize error logging
C3	Initialize error display function
C4	Initialize system error handler
C5	PnP dual CMOS (optional)
C6	Initialize notebook docking (optional)
C7	Initialize notebook docking late
C8	Motorola check (optional)
C9	Extended checksum (optional)
CA	Redirect Int 15h to enable remote keyboard
CB	Redirect Int 13 to Memory Technologies Devices such as ROM, RAM, PCMCIA, and serial disk
CC	Redirect Int 10h to enable remote serial video
CD	Re-map I/O and memory for PCMCIA
CE	Initialize digitizer and dispaly message

Post Code	Description
D2	Unknown interrupt
	The following are for boot block in Flash ROM
E1	Initialize the bridge
E2	Initialize the CPU
E3	Initialize the system timer
E4	Initialize system I/O
E5	Check recovery boot
E6	Checksum BIOS ROM
E7	Go to BIOS
E8	Set Huge Segment
E9	Initialize Multi Processor
EA	Initialize OEM special code
EB	Initialize PIC and DMA
EC	Initialize Memory type
ED	Initialize Memory size
EE	Shadow Boot Block
EF	System memory test
F0	Initialize interrupt vectors
F1	Initialize Run Time Clock
F2	Initialize video
F3	Initialize System Management Menager
F4	Output one beep
F5	Clear Huge Segement
F6	Boot to mini DOS
F7	Boot to Full DOS
E1	Initialize the bridge
E2	Initialize the CPU
E3	Initialize the system timer
E4	Initialize system I/O
E5	Check recovery boot

Post Code	Description
E6	Checksum BIOS ROM
E7	Go to BIOS
E8	Set Huge Segment
E9	Initialize Multi Processor
EA	Initialize OEM special code
EB	Initialize PIC and DMA
EC	Initialize Memory type

5

Devices' Features and Data Paths

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Block Diagram

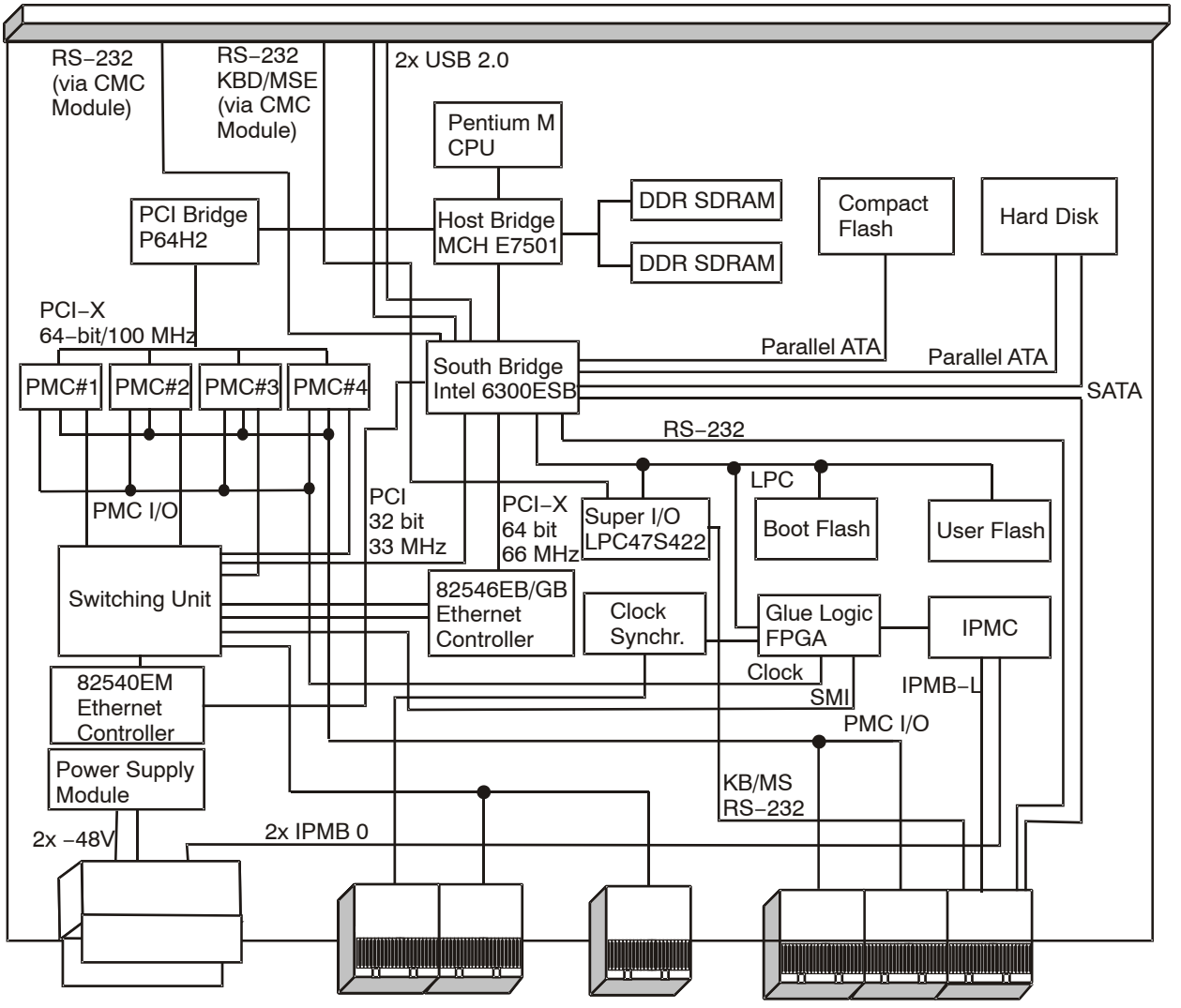

Figure 34: *Base Board Block Diagram*

CPU

The used Central Processing Unit (CPU) is a Pentium M processor. The CPU provides 32 kBytes of on–die data and instruction cache as well as two MByte L2 cache.

An on–die temperature sensor measures the CPU temperature. It is connected to the blade's Intelligent Peripheral Management Controller (IPMC). This way software can monitor the CPU temperature via IPMI.

Host Bridge

The used host bridge is an Intel E7501 Memory Controller Hub (MCH) device. It is part of the Intel Plumas chipset and provides bus control signals, address and data paths for transfers between the CPU front side bus, main memory and the four hub interfaces provided by the host bridge.

Host Interface

The host interface supports a 64–bit wide data bus and a 32–bit wide address bus. The data bus is quadpumped and runs at 100 MHz, resulting in a total bandwidth of 3.2 GB/s. The memory bus is double pumped and supports an address range of up to 4 GByte. Its bandwidth is 200 Mb/s per data line resulting in a total bandwidth of 128 x 200MB/S = 3.2GB/s.

Memory Interface

The memory interface is a 144–bit wide SDRAM interface supporting 64, 128, 256 and 512 MBit DDR SDRAM technology. The bus speed is 100 MHz running synchronously to the front side bus. Additionally ECC is supported.

Although theoretically up to 16 GByte are supported by the memory interface, the actual maximum memory size is limited to 4 GByte due to the CPU's 32–bit address bus.

Hub Interfaces

The Host Bridge provides the four hub interfaces A, B, C and D.

Hub interface A is quad pumped, 8–bit wide and runs at 66 MHz. It is connected to the South Bridge and provides a maximum data transfer rate of 266MByte/s. Parity protection is provided for hub interface A. Any parity errors are detected by the host bridge and reported to the South Bridge, which in turn generates an NMI.

The hub interfaces B, C and D are octal pumped, 16–bit wide and run at 66 MHz. The maximum data transfer rate provided by each hub interface is 1.066 GByte/s.

ECC protection is provided for hub interfaces B, C and D. Any ECC errors are detected by the host bridge and reported to the South Bridge, which in turn generates an NMI.

South Bridge

The used South Bridge is an Intel 6300ESB I/O controller hub device. It provides the interface between the Host Bridge and the legacy I/O. Integrated into the South Bridge are:

- Two 8237 DMA controllers
- One 8254 counter timer
- Interrupt controller
- Real-time clock
- Watchdog

The interfaces provided by the South Bridge include:

- Hub interface 1.5
- PCI 2.2 interface
- PCI-X 1.0 interface
- Two parallel ATA interfaces
- Two serial ATA interfaces
- Two serial RS-232 interfaces
- Four USB interfaces
- LPC interface
- SMBus interface

Interrupt Controller

The interrupt controller residing in the South Bridge is 8259A-compliant and runs in PIC mode.

The interrupts of the four PMC slots are merged and are routed through an FPGA to the interrupt controller where they are mapped to ISA compatible interrupts.

The interrupt controller is also able to generate CPU Non-Maskable Interrupts (NMIs). Possible sources of NMIs are:

- Memory ECC and parity errors

- Hub interface ECC and parity errors
- PCI bus parity errors

Real–Time Clock

The Real–Time Clock (RTC) resides inside the South Bridge and is sourced by an external 32.768 crystal providing a frequency tolerance of 20 ppm. The RTC provides 242 bytes backed–up CMOS RAM and is fully compliant to:

- DS1287
- MC14618
- Y2K
- PC87911

Watchdog

The Southbridge incorporates a two–stage watchdog timer. For details refer to the Intel 6300ESB I/O controller documentation. On expiry, the watchdog is able to issue a blade reset.

PCI–X Interface

The PCI–X interface is 64–bit wide and runs at 66 MHz. It is compliant to the PCI–X 1.0 specification. On the board 3.3V signalling level is used and an 82546EB/GB dual Ethernet controller is connected to the PCI–X interface.

Parallel ATA Interfaces

The South Bridge provides two separate parallel Advanced Technology Attachment (ATA) interfaces: one primary and one secondary parallel ATA interface. Both interfaces support all Programmed I/O (PIO) modes as well as all Direct Memory Access (DMA) modes up to Ultra ATA/100. The combined parallel and serial ATA interface traffic is indicated by a face plate LED.

Primary Parallel ATA Interface

The primary parallel ATA interface is connected to an on–board 2.5″ hard disk which can be mounted on the blade. The hard disk operates as IDE master.

Secondary Parallel ATA Interface

The secondary parallel ATA interface is connected to an on-board CompactFlash connector which supports CompactFlash cards of type I and II. An inserted card runs in true IDE mode and is master on the secondary parallel ATA interface.

USB Interfaces

The South Bridge provides four USB interfaces. Two are routed to the blade's face plate and two to the rear transition module. All interfaces are compliant to the USB 2.0 standard.

PCI Interface

The South Bridge provides a 32-bit/33 MHz PCI interface that is compliant to the PCI 2.2 specification. Up to four external PCIbus master devices are supported and a 3.3V signaling level is used.

Serial ATA Interfaces

The South Bridge provides two Serial Advanced Technology Attachment (SATA) interfaces which are compliant to the SATA 1.0 specification and support a data transfer rate of up to 1.5GByte/s. One interface is routed to the Zone 3 connector and is accessable via an installed RTM. One interface is routed to an on-board SATA connector to which a SATA hard disk can be connected.

Serial RS232 Interfaces

The South Bridge provides two serial full-duplex RS232 interfaces. Supported baud rates are: 600, 1200, 2400, 4800, 9600, 19200, 38400 and 115200 kb/s. Both serial interfaces are +/- 15 KV ESD protected.

Both interfaces correspond to the blade's serial interface ports 1 and 3. Serial interface port 1 is routed via a zone 3 connector to an installed RTM. Serial interface port 3 is accessible via an installed CMC module. The BIOS maps the serial interfaces ports to the desired I/O addresses (COM ports) and interrupts.

LPC Interface

The South Bridge provides a 4-bit wide Low Pin Count (LPC) interface running at 33 MHz. It has the following devices attached to it:

- Super I/O

- Boot flash
- User flash
- Glue Logic FPGA

SMBus Interface

The following table lists all devices which are connected to the South Bridge via its SMBus interface:

Device Name	Device Type	SMBus Address
SPD EEPROM (contains memory configuration data of memory module, used by BIOS)	24C02	0xA0
SPD EEPROM (contains memory configuration data of memory module, used by BIOS)	24C02	0xA1
Host Bridge	Intel E7501	0x60
PCI bridge	P64H2	0xC0
South Bridge	6300ESB	0x44

Super I/O

The used Super I/O is a Standard Microsystems Corporation LPC47S422 device. It provides the following interfaces:

- Two serial interfaces
- Floppy disk interface
- Keyboard/Mouse interface
- Parallel interface

Serial Interfaces

The Super I/O device provides two serial full-duplex RS232 interfaces. Supported baud rates are: 600, 1200, 2400, 4800, 9600, 19200, 38400 and 115200 kb/s. Both serial interfaces are +/- 15 KV ESD protected.

Both interfaces correspond to the blade's serial interface ports 2 and 4. Serial interface port 2 is routed via a zone 3 connector to an installed RTM. Serial interface port 4 is accessible via an installed CMC module. The BIOS maps the serial interface ports to the desired I/O addresses (COM ports) and interrupts.

Floppy Disk Interface

The floppy disk interface is unused on the blade.

Keyboard/Mouse Controller

The Super I/O integrates an 8042H compatible keyboard/mouse controller. The corresponding interfaces are accessible via RTM and CMC debug module.

Parallel Interface

The parallel interface is unused on this blade.

Flash Devices

The blade provides two redundant boot flash devices: one default boot flash and one backup boot flash. During blade production, both flashes are programmed with identical BIOS images. The presence of two redundant flash devices allows for remotely updating BIOS images from the operating level without interrupting running processes and without being affected by possibly corrupt BIOS images. The backup boot flash, furthermore, can be used to store customized images. Note that in this case the redundant BIOS feature is no longer available.

Both flash devices are Intel-compatible firmware hubs that are connected to the LPC interface of the South Bridge. Each flash device has a unique four bit LPC device ID. Bit 1 to 3 of the device ID are fixed to 0. Bit 0 is controlled by a boot flash select signal provided by the IPMC in such a way that bit 0 of one flash is set to 0 while bit 0 of the other flash is set to 1 and vice versa. The following figure shows the implementation on hardware-level.

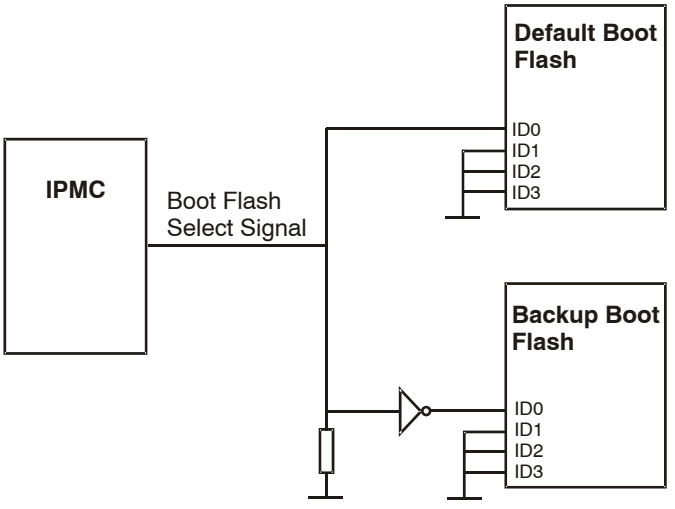

Figure 35: *Boot Flash LPC Device ID Control*

The blade' s CPU always boots from the boot flash with the LPC device ID 0. Thus the boot flash select signal of the IPMC allows to select the flash device that the CPU is to boot from.

An IPMI Set System Boot Options command allows to control the boot flash select signal and thus select between the default and backup boot flash as device to boot from. For details refer to the *PENT/ATCA-715/717/7105/7107: Control via IPMI Programmer's Guide* which can be downloaded from the former Force Computers S.M.A.R.T. server or the Motorola literature catalog.

By default, the data/instruction areas of the default and backup boot flash are writable. This is necessary because during booting the BIOS writes some configuration data back to

some reserved spaces in the data/instruction area. The boot block of default and backup boot flash are writeable per default, too. The on–board switches SW4–1, SW4–2 and SW4–4 allow to enable/disable the write–protection of both default and backup boot flash as well as the data/instruction area of the backup boot flash.

FPGA

The FPGA implements the following functions:

- LPC interface
- IPMC interface
- Clock synchronization extensions
- Reset controller
- Interrupt routing unit
- Miscellaneous glue logic
- Ethernet switch interface

The FPGA loads its configuration stream from one of two EEPROMs which are connected to the FPGA. One EEPROM serves as default, the second as backup EEPROM. The IPMC controls which EEPROM the configuration stream is loaded from. After IPMC startup the FPGA loads its configuration stream from the default EEPROM. An IPMI System Boot Options command allows to select between default and backup EEPROM. For details about switching between default and backup FPGA refer to the *PENT/ATCA-715/717/7105/7107: Control via IPMI Programmer's Guide* which can be downloaded from the Motorola literature site.

LPC Interface

The LPC interface is compliant to the Intel LPC specification 1.1 and connects the FPGA to the South Bridge.

IPMC Interface

The FPGA is connected to the on-board IPMC and implements the following IPMC related features:

- Two Block Transfer interfaces
- Port 80 register
- IPMC extensions

Block Transfer Interfaces

Two Block Transfer interfaces (BT) reside inside the FPGA. Each provides one control and status register, two 64-byte FIFOs and an interrupt mask register. Both BT interfaces are

compliant to the IPMI specification V1.5 Rev. 1.0 and share one Interrupt Source register. The first BT interface is used as the only System Interface and uses IPMI channel 0x0F. The second BT interface uses IPMI channel 0x06.

Port 80 Register

The FPGA provides an 8-bit wide register to store POST codes. The register is located at I/O address 80_{16}.. It is only readable for the IPMC and read-writeable for the host. The IPMC polls this register to monitor the boot up sequence of the board. The content of the port 80 register can also be obtained and read via IPMI.

IPMC Extensions

The FPGA implements three registers which are only visible for the IPMC. These registers reflect the following:

- CPU core voltage identifier
- Frame signal on LPC bus
- System and parity errors on PCI buses
- Enabling/disabling of backplane signals used for electronic keying
- Alert signals

Clock Synchronization Extensions

The FPGA contains extensions which are related to the AdvancedTCA clock synchronization feature. These extensions include:

- Registers accessible via host and IPMC for controlling and monitoring clock synchronization
- SPI interface for controlling DPLL device
- Programmable clock divider

For further details refer to section "Clock Synchronization Interface" on page 124 and section "Clock Synchronization Interface Registers" on page 144.

Reset Controller

The FPGA contains part of the blade's reset logic. Furthermore it provides two registers which allow to determine the source of the last reset issued and to mask resets.

Reset Types

Two different types of resets are possible: hard resets and soft resets.

During a hard reset all internal registers, state machines and caches of the CPU are reset. Furthermore all on–board PCI devices as well as the host bridge are reset.

During a soft reset the CPU is reset, with the exception of the internal caches and state machines

Reset Sources

The following table lists all possible reset sources and the corresponding reset types.

Table 10: *Reset Sources*

Reset Source	Hard Reset	Soft Reset
Software reset	x	x
Watchdog inside Southbridge	x	
Power–up reset	x	
Face plate reset key	x	
RTM reset	x	
IPMC reset	x	
Keyboard reset		x

Interrupt Routing Unit

The FPGA is used for fixed interrupt routing on the blade.

All interrupts from PCI devices are routed via the FPGA to the South Bridge. All other interrupts are routed to the Super I/O device from where they are routed to the South Bridge.

Miscellaneous Glue Logic

The miscellaneous glue logic includes:

- Serial interface
- Reset mask and source register
- Flash control register
- PMC status register
- Shut–down register

- LEDs
- Version register

Serial Interface

The FPGA provides routing options of one of the two serial interfaces provided by the Southbridge. This feature is intended for Motorola-internal purposes and should be ignored. .

Reset Mask and Source Register

The FPGA provides two registers which allow to obtain the last reset source and to mask resets. See section "Reset Registers" on page 139.

Flash Control Register

The FPGA provides one register which allows to monitor the boot and user flash write-protection status as well as to control the write-protection of the boot flash boot block. See section "Flash Control and Status Register" on page 141

PMC Status Register

The FPGA provides one register which allows to monitor the status of the four PMC sites. See section "PMC Status Register" on page 143

Shut-Down Register

The FPGA provides one register which allows to control the blades' FRU-EN signal. See section "Shut Down Register" on page 143

LEDs

The FPGA provides a register to control the HDD LED available at the face plate. This LED indicates the combined parallel and serial ATA activity or is operated in user LED mode. See section "LED Control Register" on page 142.

Version Register

This register allows to obtain the current FPGA version. See section "Version Register" on page 147.

Intelligent Platform Management Controller

The blade provides an Intelligent Platform Management Controller (IPMC) unit based an the 8-bit Atmel ATmega AVR microcontrollers. The IPMC is fully compliant to the IPMI V1.5 standard and provides the following interfaces:

- IPMB0A and IPMB0B available via the backplane
- IPMB-L connected to rear transition module
- I2C interfaces connected to on-board PMCs slots and sensors
- Analog-to-Digital Conversion (ADC)interfaces connected to on-board sensors
- Digital I/O interfaces connected to on-board sensors

One of the main tasks of the IPMC is to control the power up and power down of the blade. For this purpose the IPMC is connected to the on-board power supply module via control and status lines. Various on-board IPMI sensors provide detailed information on the current power status of the blade to any interested party connected to the IPMI network.

The following figure gives an overview of the IPMI structure used on-board.

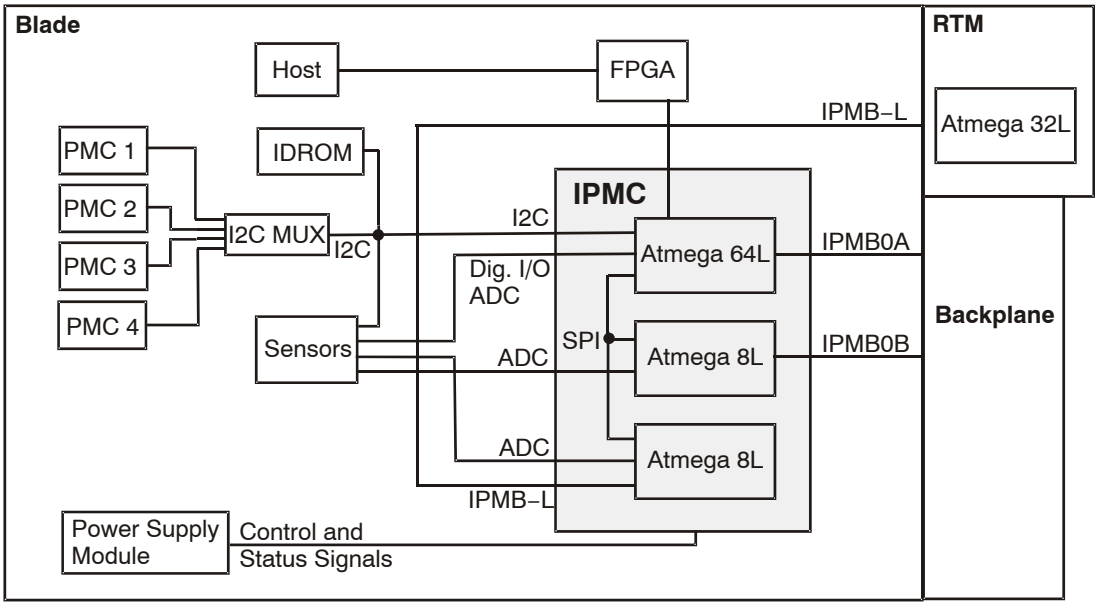

Figure 36: *IPMI Structure*

For details about accessing the IPMC via IPMI commands as well as Sensor Data Records (SDRs) and Field Replacable Unit (FRU) information provided by the blade, refer to the *"PENT/ATCA-715/717/7105/7107 Control via IPMI Programmer's Guide"* which can be downloaded from the Motorola literature catalog.

Sensors

The blade provides various sensors which are accessible via IPMI. Some of these sensors measure on–board temperatures. Their names and locations are shown in the following figure.

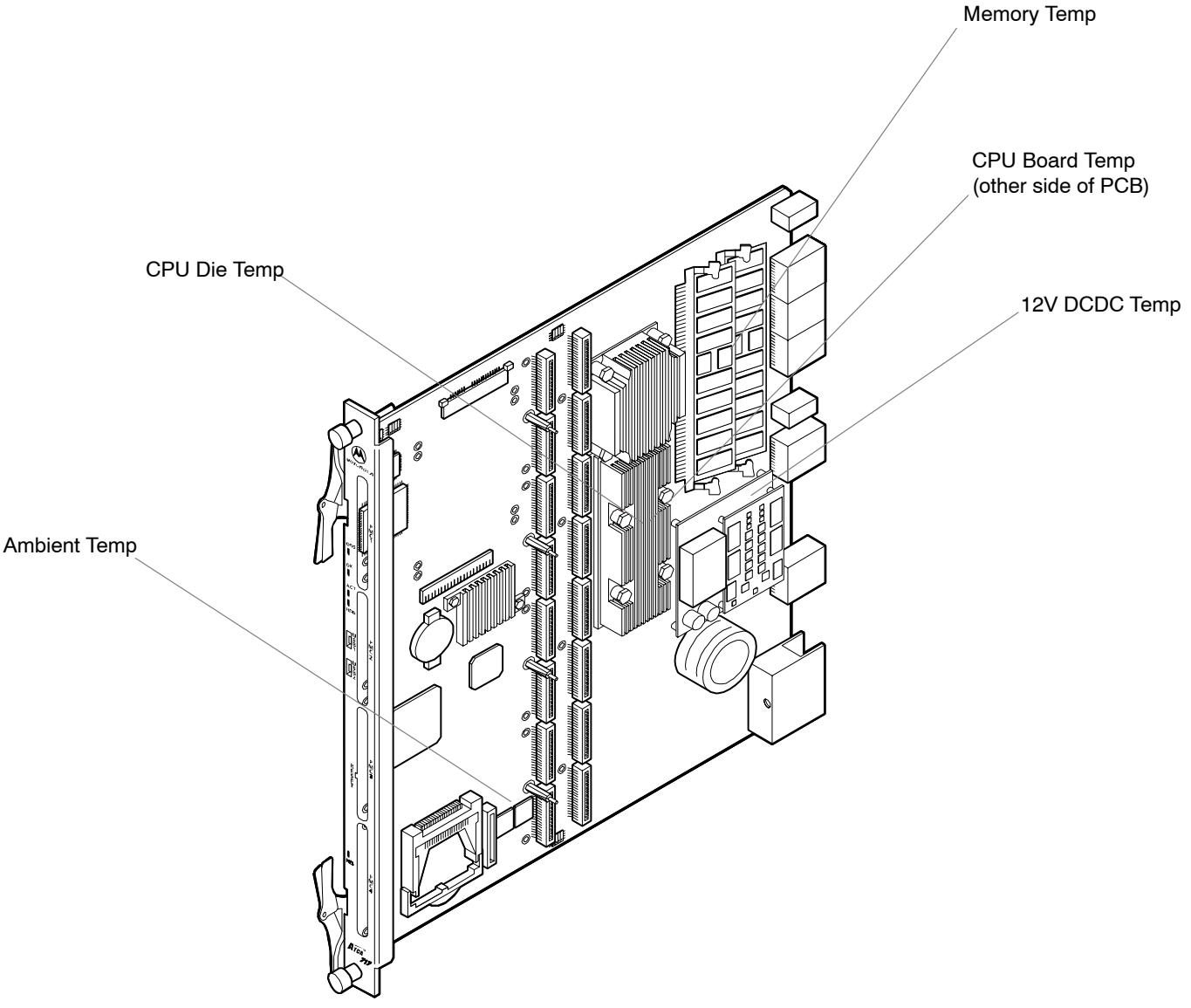

Figure 37: *IPMI Temperature Sensors*

Other sensors available on–board include voltage sensors and sensors which provide particular status information. A summary of all sensors is given in the following table.

Table 11: *On-board Sensors Accessible via IPMI*

Sensor Name	Type of Measurement	What Does It Measure?	Sensor Type	Availability
Ambient Temp	Temperature	Ambient temperature near Compact flash connector	Analog	Always
Memory Temp	Temperature	Temperature of on-board memory	Analog	Always
CPU Board Temp	Temperature	Board temperature near the CPU	Analog	Always
CPU Die Temp	Temperature	CPU temperature	Analog	Always
Voltage +1.8V	Voltage	+1.8V voltage level	Analog	While Payload powered ON
Voltage +1.5V	Voltage	+1.5V voltage level	Analog	While Payload powered ON
Voltage +3.3V	Voltage	+3.3V voltage level	Analog	While Payload powered ON
Voltage +5V	Voltage	+5V voltage level	Analog	While Payload powered ON
Voltage +12V	Voltage	+1.2V voltage level	Analog	While Payload powered ON
Voltage +1.05V	Voltage	+1.05V voltage level	Analog	While Payload powered ON
Voltage +1.25V	Voltage	+1.25V voltage level	Analog	While Payload powered ON
Mem Volt +1.2V	Voltage	+1.2V voltage level of the memory termination voltage	Analog	While Payload powered ON

Sensor Name	Type of Measurement	What Does It Measure?	Sensor Type	Availability
Mem Volt +2.5V	Voltage	+2.5V voltage level of the memory supply voltage	Analog	While Payload powered ON
Sw Volt +1.2V	Voltage	+1.2V voltage level of Ethernet switch chip	Analog	While Payload powered ON
CPU THERM TRIP	Temperature	CPU has stopped execution because CPU temperature has exceeded safe limits	Discrete	While Payload powered ON
ICH PROC HOT	Temperature	CPU temperature has reached maximum safe operating limit	Discrete	While Payload powered ON
FPGA PROGRAMMED	Status	FPGA programming status	Discrete	While Payload powered ON
Sw Volt +2.5V	Voltage	+2.5V voltage level of Ethernet switch chip	Analog	While Payload powered ON
CPU CORE Volt	Voltage	CPU core voltage level	Discrete	While Payload powered ON
715 Watchdog	Status	Watchdog status	Discrete	Always
715 RTM HotSwap	Status	RTM presence	Discrete	Always
715 IPMB0 State	IPMB status	ATCA IPMB0	Discrete	Always
715 POST Code	Status	POST status	Discrete	While Payload powered ON
PCI BUS ERR	Status	PCI bus status	Discrete	While Payload powered ON

Sensor Name	Type of Measurement	What Does It Measure?	Sensor Type	Availability
715 FPGA Version	Version	FPGA version of ATCA–715	Discrete	Always after payload has first been powered ON
FW Revision ISC0	Revision	Revision of the Intelligent Slave Controller 0 (ISC0) firmware	Discrete	Always
FW Revision ISC1	Revision	Revision of the Intelligent Slave Controller 1 (ISC1) firmware	Discrete	Always
715 IPMC	Status	IPMC status	Discrete	Always
SYS FW PROGRESS	Status	BIOS boot progress	Discrete	While Payload powered ON
Boot Error	Status	BOOT error	Discrete	While Payload powered ON
Supply Current	Current	12V payload current	Analog	While payload powered ON
12V DCDC Temp	Temperature	Temperature at 12V DC/DC converter	Analog	While payload powered ON

For further details refer to the *"PENT/ATCA–715/717/7105/7107 Control via IPMI Programmer's Guide"* which can be downloaded from the Motorola literature catalog.

I2C Addresses

The blade provides one IDROM which is attached to the IPMC via an I2C bus. The I2C address of the IDROM is 0xA0.

Clock Synchronization Interface

AdvancedTCA systems provide a telecom clock synchronization interface which allows to synchronize elements within a telecommunication network. The telecom clock synchronization interface consists of three redundant clock buses (CLK1, CLK2 and CLK3) which are available at the system backplane. Each clock bus is implemented as a differential pair of MDS/LDS signals which connects to each system slot.

In compliance with the AdvancedTCA PICMG 3.0 specification, CLK1 and CLK2 are used as system clocks and CLK3 is used as reference clock.

The blade provides a clock synchronization building block which allows to synchronize the four on-board PMC modules to the system clock and to derive a reference clock. The main components of the clock synchronization building block as well as the main signal paths are shown in the following figure.

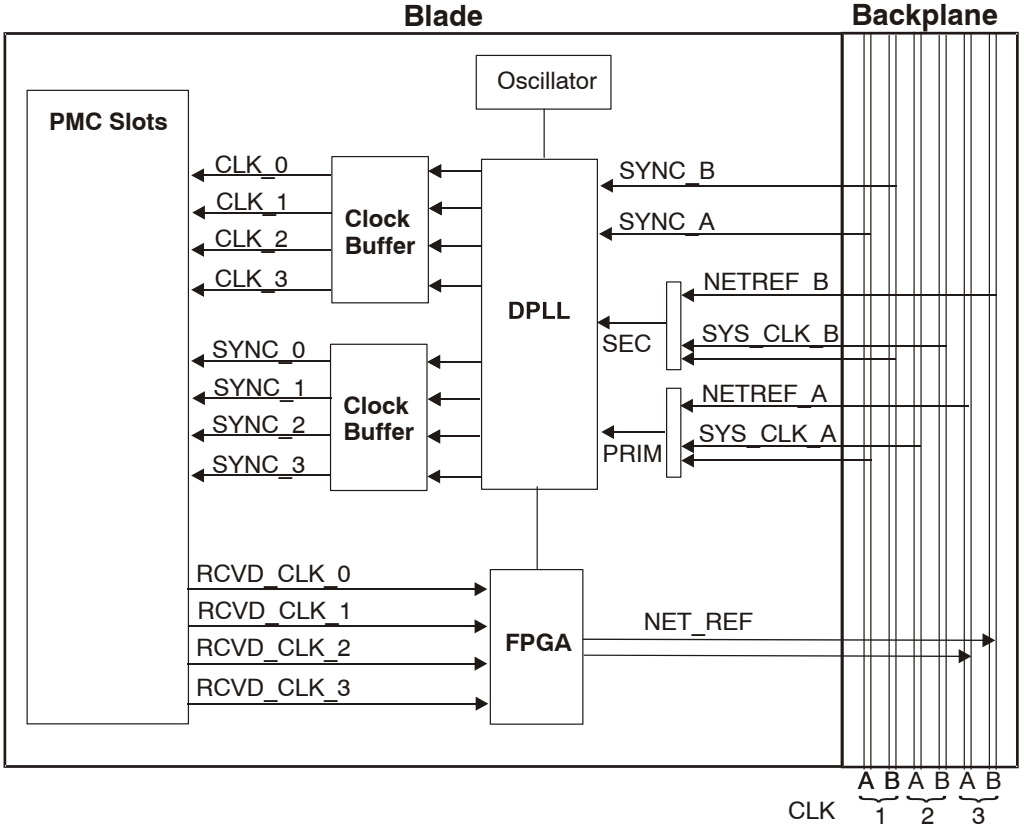

Figure 38: *Clock Synchronization Building Block*

The key component of the clock synchronization building block is the DPLL device ACS8525 from Semtech. Its main features include:

- Software programmable output clock synthesis (CLK_0, 1, 2, 3)

- 8 kHz frame clock/pulse with programmable pulse width and polarity (SYNC_0,1,2,3))
- Automatic hit-less switch-over if one system clock fails
- Activity monitor for system clocks
- Phase build-out for output clock phase continuity during switch-over
- Meets jitter requirements up to OC-3 line rates
- Programmable reference clock divider

The DPLL is clocked by an external oscillator running at 12.8 MHz. Two clock buffers provide a separate clock and synchronization signal for each of the four on-board PMC sites. The FPGA contains extensions which are related to the clock synchronization building block. Some of these extensions include registers that are accessible via the host and which allow to control and monitor the functionality of the clock synchronization building block. For details refer to section "Clock Synchronization Interface Registers" on page 144.

Power Supply Module

The blade is fed via two redundant -48V inputs. Both are converted via a DC/DC converter to an intermediate voltage of +12V. This voltage, in turn, is converted via further DC/DC converters to on-board voltages which are used by the on-board devices. A -48V/+3.3V DC/DC converter converts the -48V input voltage to +3.3V which is used to feed the IPMC and power-up logic.

The blade's power up and power down cycles are under full control of the IPMC. It controls both the -48V/+12V DC/DC converter as well as power-up logic which controls the remaining on-board DC/DC converters. If the IPMC detects a failure on any of the local on-board voltages, it shuts off the entire blade power.

The blade's power supply structure is shown in the following figure.

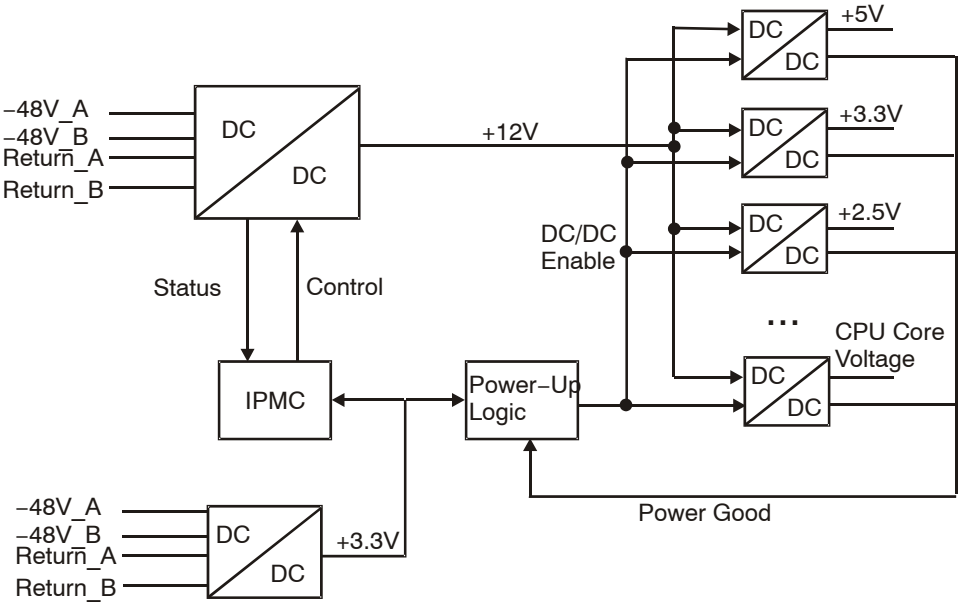

Figure 39: *Blade Power Supply Structure*

PCI Bridge P64H2

The Intel P64H2 PCI bridge provides two PCI/PCI-X interfaces. Each interface is connected to two PMC sites. The P64H2 device supports peer-to-peer communication between the two PCI/PCI-X interfaces. This way no host intervention is required when PMC sites connected to different PCI/PCI-X interfaces communicate with each other. In PCI mode up to 533 MHz/s transfer rate is possible, in PCI-X up to 800 MByte/s.

Switching Unit

The on-board switching unit is based on the Marvell 98DX160 Ethernet layer 2+ switch and provides switching functionality between on-board Ethernet ports, PMC sites and the backplane interfaces. It provides 16 Ethernet switching ports as well as one Serial Management interface (SMI) and one additional Ethernet port for configuration.

Features

Important features of the switching unit are:

- 2 MByte internal memory
- Host management interface
- Support for 1000 MII/GMII/RGMII and 1000Base-X
- Manual and auto-negotiation
- Support for jumbo frame length of 10KByte packets
- On-chip 4K MAC address table
- 4K VLANs with 256 active VLANs
- Flexible VLAN assignment for protocol- port- and tag-based VLANs

Management Interface

The switching unit provides two management interfaces towards the host: one slave Serial Management Interface (SMI) and one CPU Ethernet port. The SMI interface is accessible via FPGA registers and supports read and write accesses to address mapped entities. The CPU Ethernet port is constituted by an Intel 82540EM GBit Ethernet controller which is connected to the PCI interface of the blade's South Bridge.

Routing Options

The blade is designed to support dual-dual star backplanes. However, the currently available blade variants support only dual star backplanes. Ask your local Motorola representative for more information on available blade variants and switch options.

Starting with blade revision 1.2, the blade provides support for PICMG 3.1 Option 2. This is achieved by configuring two fabric interface ports as one 2 GBit Ethernet trunc. Details are given below.

At blade start-up the Ethernet switch reads a serial PROM which contains switch configuration information such as predefined Virtual Local Area Networks (VLANs).

The following table shows how the Ethernet interfaces are distributed across the 16 Ethernet switch ports.

Table 12: *Ethernet Switching Unit –Ethernet Port Distribution*

Interfaces	Number of Ethernet Ports
PMC sites	2 x 1 and 2 x 2
Host Ethernet	2 x 1
Base interface	2 x 1
Fabric interface	2 x 1 and 2 x 2
Update channel interface	–
Total	16

Four VLANs are predefined. Each backplane Ethernet interface is assigned to one separate VLAN. On–board Ethernet interfaces, however, belong to more than one VLAN.

The fabric interfaces are attached to tagged VLANs, and the base interfaces to untagged VLANs.

The following figure illustrates the VLAN configuration.

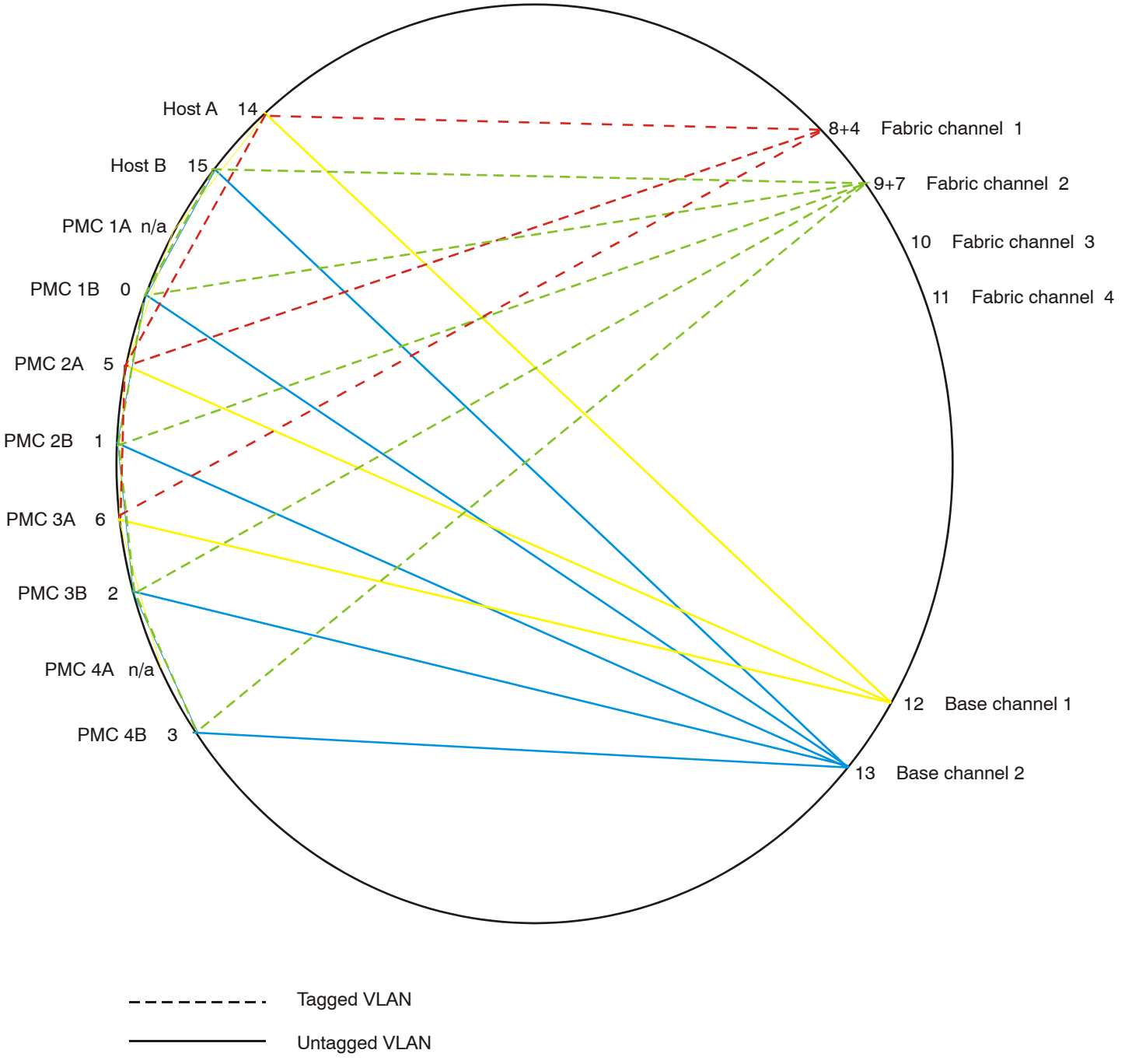

Figure 40: *VLAN Configuration*

The following table summarizes the Ethernet switch configuration by listing Ethernet interfaces, port numbers, VLAN IDs and Ethernet types.

Note: Only port 0 and 1 of the fabric channels are used.

Table 13: *Ethernet Switching Unit – Port Assignment*

Switching Unit Port Number	Destination	Interface Type	ID of Untagged VLAN	ID of Tagged VLAN
0	PMC 1B	1000BaseT	3	5
1	PMC 2B	1000BaseT	3	5
2	PMC 3B	1000BaseT	3	5
3	PMC 4B	1000BaseT	3	5
4	Fabric channel 1T	1000BaseBX	–	4
5	PMC 2A	1000BaseT	2	4
6	PMC 3A	1000BaseT	2	4
7	Fabric channel 2T	1000BaseBX	–	5
8	Fabric channel 1	1000BaseBX	–	4
9	Fabric channel 2	1000BaseBX	–	5
10	Fabric channel 3	1000BaseBX	–	–
11	Fabric channel 4	1000BaseBX	–	–
12	Base channel 1	1000BaseT	2	–
13	Base channel 2	1000BaseT	3	–
14	Primary base board/82546EB/GB Ethernet controller	1000BaseBX	2	4
15	Secondary base board/82546EB/GB Ethernet controller	1000BaseBX	3	5

6

Maps and Registers

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I/O and Memory Maps

The following table shows the blade's main address map.

Table 14: *Memory Address Map*

Base Address	Size	Device
$FFF0.0000_{16}$	1 MByte	Boot Flash
$FFE0.0000_{16}$	1 MByte	User Flash
0000.0000_{16}	Up to 4GByte	Main Memory

The I/O addresses of all on-board functional units are listed below.

Table 15: *I/O Address Map*

Device	Base Address
DMA Controller #1	$000_{16}...01F_{16}$ and $080_{16}...09F_{16}$
Interrupt Controller #1	$020_{16}...03F_{16}$
Timer	$040_{16}...05F_{16}$
Keyboard/Mouse	$060_{16}...06F_{16}$
Real-Time Clock	$070_{16}...07F_{16}$
Port 80	080_{16}
Interrupt Controller 2	$0A0_{16}...0BF_{16}$
DMA Controller 2	$0C0_{16}...0DF_{16}$
IPMI Block Transfer Interface 1	$0E4_{16}$ - $0E6_{16}$
IPMI Block Transfer Interface 2	$0E8_{16}$ - $0EA_{16}$
Glue Logic FPGA Index Register	100_{16} – 101_{16}
Ethernet Switch Management Interface	$150_{16}...155_{16}$
Secondary Parallel ATA	$170_{16}...178_{16}$ or 376_{16}, 377_{16}
Primary Parallel ATA	$1F0_{16}...1F8_{16}$ or $3F6_{16}$, $3F7_{16}$
Floppy Disk	$3F0_{16}...3F5_{16}$
COM 1	$2F8_{16}...2FF_{16}$ or $2E8_{16}...2EF_{16}$ or $3E8_{16}...3EF_{16}$ or $3F8_{16}...3FF_{16}$
COM 2	$2F8_{16}...2FF_{16}$ or $2E8_{16}...2EF_{16}$ or $3E8_{16}...3EF_{16}$ or $3F8_{16}...3FF_{16}$

Device	Base Address
COM 3	$2F8_{16}...2FF_{16}$ or $2E8_{16}...2EF_{16}$ or $3E8_{16}...3EF_{16}$ or $3F8_{16}...3FF_{16}$
COM 4	$2F8_{16}...2FF_{16}$ or $2E8_{16}...2EF_{16}$ or $3E8_{16}...3EF_{16}$ or $3F8_{16}...3FF_{16}$

Hardware Interrupts

The following table lists the blade's hardware interrupts and the corresponding interrupt sources.

Note: All interrupts marked with an asterisk (*) must not be used for PCI interrupt routing.

Table 16: *Hardware Interrupts*

Interrupt	Interrupt Source
IRQ0*	Timer
IRQ1*	Keyboard
IRQ2*	Input of interrupt controller #2
IRQ3	COM 2 or COM 4
IRQ4	COM 1
IRQ5	COM 3
IRQ6	IPMI Block Transfer interface
IRQ7	PCI
IRQ8*	Real time clock
IRQ9	PCI
IRQ10	PCI
IRQ11	PCI
IRQ12	Reserved or Mouse (PS/2)
IRQ13*	Coprocessor
IRQ14	Reserved or primary parallel ATA
IRQ15	Reserved or secondary parallel ATA

PCI Devices

The following figure shows the on-board PCI device structure.

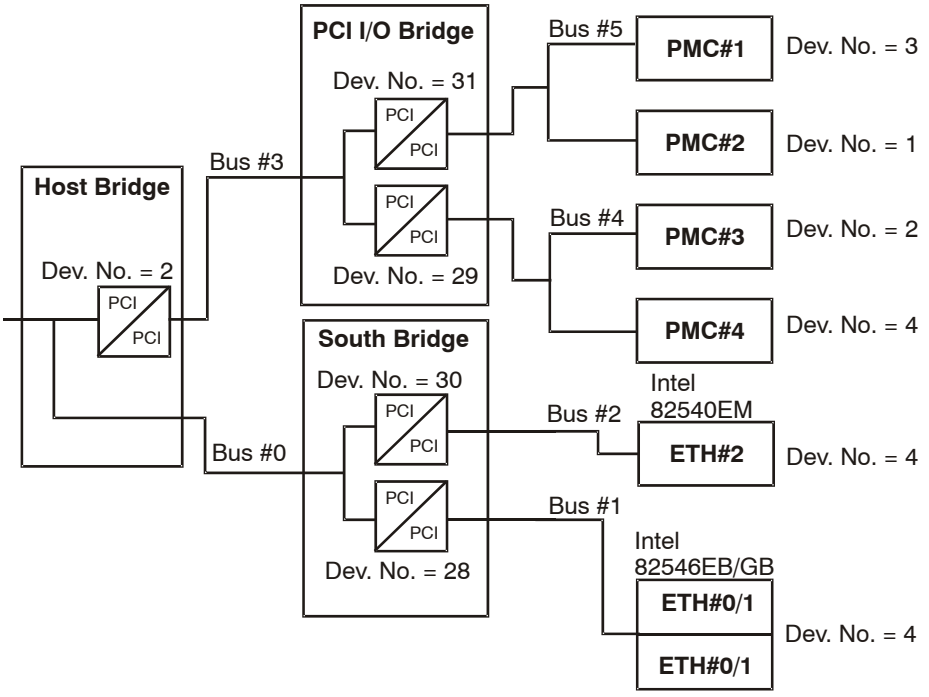

Figure 41: *PCI Structure*

The following table lists the PCI devices interrupt signals which are routed to the South Bridge. BIOS allows to map these signals to standard ISA interrupts.

Table 17: *PCI Device Interrupts*

PCI Device	PCI IRQ	Device No.	IDSEL	PCI Bus
PMC 1	PIRQA_N | PIRQB_N | PIRQC_N | PIRQD_N	3	19	5
PMC 2	PIRQA_N | PIRQB_N | PIRQC_N | PIRQD_N	1	17	5
PMC 3	PIRQA_N | PIRQB_N | PIRQC_N | PIRQD_N	2	18	4
PMC 4	PIRQA_N | PIRQB_N | PIRQC_N | PIRQD_N	4	20	4
ETH 2	PIRQC_N	4	20	2
ETH 0 | 1	PIRQA_N | PIRQB_N	4	20	1

FPGA Registers

The FPGA provides various control and status registers. Some of these registers are accessible from the CPU host via the LPC bus, some by the IPMC, others by both. In the following all registers will be described which are accessible from the CPU. These registers are listed in the following table.

Table 18: *Registers Accessible from CPU via LPC Bus*

Address Range	Data Width	Description
0xE4 – 0xE6	8 bit	IPMI Block Transfer Interface 0
0xE8 – 0xEA	8 bit	IPMI Block Transfer Interface 1
0x80	8 bit	Port 80
0x100	8 bit	Index Address Register (used for accessing further FPGA registers)
0x101	8 bit	Index Data Register (used for accessing further FPGA registers)
0x150 – 0x155	8 bit	Ethernet Switch Management Interface

The FPGA provides further registers. In order to access them, first write the index address corresponding to the register to the Index Address Register, and then perform either a read or write access on the Index Data Register. All registers that can be accessed this way are listed in the following table.

Table 19: *Index Addresses of Registers Accessible from CPU via LPC Bus*

Index Address	Data Width	Description
0x00	8 bit	Reset Source Register
0x01	8 bit	Reset Mask Register
0x02	8 bit	Flash Control and Status Register
0x03	8 bit	LED Control Register
0x04	8 bit	PMC Status Register
0x05	8 bit	Shut Down Register
0x30 – 0x3F	8 bit	Clock synchronization interface
0x40	8 bit	Serial PROM Update Register
0x41	8 bit	Access Control Register
0xFF	8 bit	Version Register
All other	8 bit	Reserved

IPMI Block Transfer Interface Registers

The host can access the IPMC via the two Block Transfer (BT) Interfaces 0 and1. Both are fully compliant to the IPMI specification V1.5. Each BT interface provides the following registers.

Table 20: *IPMI Block Transfer Interface Registers*

Address Offset	Data Width	Description
0x00	8 bit	Control and status register
0x01	8 bit	Buffer Register
0x02	8 bit	Interrupt mask register

Control and Status Register

This register is used by the IPMC and the host CPU for various control functions.

Buffer Register

This register provides access to an IPMC–to–Host and Host–to–IPMC buffer. The buffer has a size of 64 bytes and contains command streams between host and IPMC.

Interrupt Mask Register

The host uses this register to mask interrupts generated by the IPMC.

Port 80 Register

This read–only 8–bit wide register, which is located at the I/O address 80_{16} stores the results obtained from the POST (Power On Self Test).

Ethernet Switch Management Registers

The following registers consitute an Ethernet management interface accessible by the host. The registers allow to configure and control the operation of the on–board Ethernet switch. The Ethernet management interface conforms to the IEEE 802.3 management draft standard. The base address of these registers is 0x150.

Table 21: *Ethernet Switch Management Registers*

Address Offset	Register
00_{16}	Command and Status Register
01_{16}	PHY address register

Address Offset	Register
02_{16}	Lower data register
03_{16}	Upper data register
04_{16}	Clock divider register
05_{16}	I2C Control and Status Register

Command and Status Register

This register controls the transfer of configuration data to and from the Ethernet switch.

Table 22: *Command and Status Register*

Bit	Description	Access
4..0	PHY internal register address	r/w
5	Command flag 0: Perform write access 1: Perform read access	r/w
6	Read Error Flag 0: PHY responds to read access 1: Error occurred	r/wc
7	Interface Status 0: Ready 1: Busy (wait until ready is indicated before initiating new access)	r

Data Registers

These registers contain the data that is read from or sent to the Ethernet switch.

Clock Divider Register

This register allows to program the frequency of the Ethernet Switch Management clock.

I2C Control and Status Register

The Ethernet switch obtains its configuration data from a PROM device that is connected to it. This register allows to access this PROM and is used for PROM updates.

Reset Registers

The blade provides two registers which are related to blade resets:

- Reset source register (index address 0x00)

- Reset mask register (index address 0x01)

The reset source register stores the source of the most recent reset. A write access clears this register.Each bit is associated with one reset source. If the bit is set to one, the corresponding reset has occurred. After a reset has occurred, this register should be cleared. Otherwise, after the next reset of another source, more than one bit is set and you may not be able to determine the most recent reset source.

Table 23: *Reset Source Register*

Bit	Signal	Description	Default	Access
0	PWR_ON	0: No reset 1: Power-on reset	1_2	r/w
1	WDG_RES	0: No reset 1: Watchdog reset	0_2	r/w
2	PB_RES	0: No reset 1: Face plate push button reset	0_2	r/w
3	PMC_RST	0: No reset 1: PMC slots reset	0_2	r/w
4	RTM_RES	0: No reset 1: RTM reset	0_2	r/w
5	CPU_RST	0: No reset 1: CPU reset issued by Host Bridge	0_2	r/w
6	PCI_RES	0: No reset 1: Legacy PCI bus reset	0_2	r/w
7	IPMI_RES	0: No reset 1: IPMC building block reset	0_2	r/w

The reset mask register allows to enable/disable particular resets. If a bit is set, the corresponding reset is enabled, otherwise it is disabled.

Note: IPMC, legacy PCI and power-on reset cannot be enabled/disabled via this register.

Table 24: *Reset Mask Register*

Bit	Signal	Description	Default	Access
0	-	Reserved	0_2	r
1	WDG_RES	Watchdog reset 0: Disabled 1: Enabled	1_2	r/w

Bit	Signal	Description	Default	Access
2	PB_RES	Face plate push button Reset 0: Disabled 1: Enabled	1_2	r/w
3	DB_RES	ITP debug reset 0: Disabled 1: Enabled	1_2	r/w
4	RTM_RES	RTM reset 0: Disabled 1: Enabled	1_2	r/w
5	PMC_RST	PMC slots reset 0 : Disabled 1: Enabled	1_2	r/w
6	–	Reserved	0_2	r
7	–	Reserved	0_2	r

Flash Control and Status Register

This register, which is accessible via the index address 0x02, indicates the status of the default and backup boot flash regarding write-protection, crisis recovery and booting. Additionally, this register allows to set the write-protection of the default boot flash data/instruction area.

Table 25: *Miscellaneous Switch Status Register*

Bit	Description	Default	Access
0	Default boot flash boot block write protection 0: Write-protected 1: Write-enabled	0_2	r
1	Default boot flash data/instruction block write protection (provided that bit 4 is set, software can set this status) 0: Write-protected 1: Write-enabled	1_2	r/w
2	Backup boot flash boot block write protection 0: Write-protected 1: Write-enabled	0_2	r
3	Backup boot flash data/instruction block write protection 0: Write-protected 1: Write-enabled	0_2	r

Bit	Description	Default	Access
4	Select status of default and backup boot flash write protection 0: Write-protection determined by on-board switches 1: Write-protection determined by this register	0_2	r
6:5	Indicates flash that is booted from 00_2: Default boot flash 01_2: Backup boot flash	00_2	r
7	Crisis recovery (indicates status of crisis recovery switch) 0: Crisis recovery 1: Normal operation	1_2	r

LED Control Register

This register, which is accessible via the index address 0x03, allows to control the bicolor face plate HDD LED. This LED can be operated in parallel/serial ATA status indication mode and user mode. Toggling between both modes is possible via this register.

In parallel/serial ATA status indication mode the LED shines GREEN and indicates the combined activitiy of all serial and parallel ATA interfaces. In user mode, the LED can be controlled to be red, green and OFF.

Table 26: *LED Control Register*

Bit	Description	Default	Access
1..0	Controls LED in user mode 00_2: OFF 01_2: Red 10_2: Green 11_2: Reserved	01_2	r/w
2	Toggles between user mode and parallel/serial ATA status indication mode 0: User mode 1: Parallel/serial ATA status indication mode	0_2	r/w
3	General purpose output on connector P30/pin A3 0: O/P is low 1: O/P is open	1_2	r/w
6	Serial COM interface swapping 0_2: No swapping 1_2: COM 1 is swapped with COM3, and COM 2 is swapped with COM 4	1_2	r
7..5	Reserved	000_2	r

PMC Status Register

This register, which is accessible via the index address 0x04, indicates the current status of all four on-board PMC sites.

Table 27: *PMC Status Register*

Bit	Description	Default	Access
0	PMC slot 1 0: Empty 1: Populated	-	r
1	PMC slot 2 0: Empty 1: Populated	-	r
2	PMC slot 3 0: Empty 1: Populated	-	r
3	PMC slot 4 0: Empty 1: Populated	-	r
4	Routing of PCIX_PMC_INT_N interrupts 0_2: Interrupts are routed to FPGA output signals PIRQA-D_N 1_2: Interrupts are routed to FPGA output signals PXIRQ_N0-3	0_2	r/w
6:5	Reserved	000_2	r
7	Indicates if PMC slots are ready for PCI enumeration 0: Not ready 1: Ready		r

Shut Down Register

This write-only register, which is accessible via the index address 0x05, allows to pull down the FRU_EN signal to GND and thus initiate a blade power-down.

This register was introduced because the FRU_EN signal is under normal operation controlled by the IPMC. If the IPMC however is is not operating anymore, for example during a firmware upgrade, the FRU_EN signal is released and remains in the state it previously had been in. In this case it may be necessary to explicitly pull down FRU_EN via this register.

Bit	Description	Access
7:0	Pull down FRU_EN signal 00111100_2: Pull down FRU_EN	w

Clock Synchronization Interface Registers

These registers are related to the clock synchronization building block of the blade. These registers are primarily used to:

- Select system clock 1 or 2 from back plane
- Select system or reference clock for DPLL input
- Enable reference clocks A and B to the backplane
- Select recovered clock source
- Determine programmable reference clock divider value
- Determine reference clock pulse width

Note: Motorola offers a device driver to access the clock synchronization interface. Instead of directly accessing the clock synchronization interface via the registers described in this section, it is strongly recommended to use this driver. Ask your local Motorola representative for details.

The following clock synchronisation interface registers are available:

Table 28: *Clock Synchronisation Interface Registers*

Index Address	Register
30_{16}	SPI Address register
31_{16}	SPI Data register
32_{16}	DPLL Input Select and Control register
33_{16}	Reference Clock Divider register
34_{16}	Lower Reference Clock Divder register
35_{16}	Upper Reference clock Divider register
36_{16}	Reference Clock Pulse Width register

SPI Interface Registers

The used DPLL device ACS8525 from SEMTECH provides a Serial Peripheral Interface (SPI) which provides external access for device setup and controlling. Software that wishes to access the DPLL device has to first set the desired address in the SPI Address register followed by either a read or write access to the SPI data register. For details about configuring the DPLL device, refer to its data sheet.

DPLL Input Select and Control Register

Table 29: *DPLL Input Select and Control Register*

Bit	Description	Default	Access
0	Selects DPLL clock source 0: System clock 1: Reference clock	0_2	r/w
1	Selects system clock source CLK1 or CLK2 0: CLK2 1: CLK1	0_2	r/w
2	Unused	0_2	r
3	SPI interface is ready for access 0: Wait 1: SPI Ready	1_2	r
4	Enabling of 2 kHz system clock interrupt 0: Disabled 1: Enabled	0_2	r/w
5	2 kHz system clock interrupt status 0: Not active 1: Interrupt pending	0_2	r
6	Clear 2 kHz system clock interrupt Writing 0 clears the interrupt Read accesses always return 0	-	r/w
7	Reset signal for DPLL 0: Reset asserted 1: Normal operation	0_2	r/w

Reference Clock Source Register

Table 30: *Reference Clock Source Register*

Bit	Description	Default	Access
1..0	Selects clock source for reference clock 00_2: RCVD_CLK_0 01_2: RCVD_CLK_1 10_2: RCVD_CLK_2 11_2: RCVD_CLK_3	00_2	r/w
3..2	Selects interrupt rate for interrupt LCCB_INT_N clocked by 2 kHz system clock reference 00_2: 500 μs 01_2: 1 ms 10_2: 10 ms 11_2: 1 s	00_2	r/w

Bit	Description	Default	Access
4	Enable reference clock CLK3_A 0: Disabled 1: Enabled	0_2	r/w
5	Enable reference clock CLK3_B 0: Disabled 1: Enabled	0_2	r/w
6	Selects if clock divider is bypassed 0: Divide clock 1: Bypass divider	1_2	r/w
7	Selection between pulse/clock on REF_CLK output signal 0: Pulse enabled 1: Pulse disabled	1_2	r/w

Reference Clock Divider Registers

The FPGA contains a clock divider which can be used in systems where the reference clock frequency does not match the recovered clock frequency. The clock divider is able to scale down a recovered clock frequency to the desired reference clock frequency. The scale down grade can be controlled via the upper and lower reference clock divider registers described in this section. Both registers correspond to the upper and lower divider of the division factor between recovered and reference clock. The division factor can be changed by software at any time. The new division factor becomes active with any new clock cycle avoiding spikes or truncated clock cycles. A plausibility check of register values is not required.

Examples of recovered and reference clock frequencies and the corresponding division factors are given in the following table.

Table 31: *Examples of Division Factors Between Recovered and Reference Clock*

Recovered Clock Frequency	Reference Clock Frequency	Division Factor
8 KHz	8 KHz	1
1.544 MHz	8 KHz	193
2.048 MHz	8 KHz	256
19.44 MHZ	8 KHz	2430
38.88 MHz	8 KHz	4860
77.76 MHz	8 KHz	9720
19.44 MHz	19.44 MHz	1

Recovered Clock Frequency	Reference Clock Frequency	Division Factor
38.88 MHz	19.44 MHz	2
77.76 MHz	19.44 MHz	4

Note: If the division factor is 1, i.e. no clock division is done, the clock divider should be bypassed. This can be done via the reference clock source register.

Lower Divider Register

Table 32: *Lower Divider Register*

Bit	Description	Default	Access
7..0	Divider lower byte	01_{16}	r/w

Upper Divider Register

Table 33: *Upper Divider Register*

Bit	Description	Default	Access
7..0	Divider upper byte	00_{16}	r/w

Reference Clock Pulse Width Register

This register determines the width of the reference clock high pulse in numbers of recovered clock cycles. The minimum pulse width is 150ns. If the clock divider is bypassed or the reference clock frequency is not 8 kHz, no pulse is generated.

Table 34: *Reference Clock Pulse Width Register*

Bit	Description	Default	Access
7..0	Pulse width of reference clock signal	01_{16}	r/w

Serial PROM Update Register

The FPGA image is stored in two redundant PROMS.This register is used by upper layer software to control the upgrade of the FPGA image. Consult your local Motorola representative for the availability of new FPGA image versions and upgrade software.

Version Register

This register indicates the version of the FPGA. The initial value is FE_{16} and is counted down with each new release.

Table 35: *Version Register*

Bit	Description	Default	Access
7..0	FPGA version	FD_{16} (at the time of writing this guide)	r

Access Control Register

This register determines the current owner of the following interfaces:

- Clock synchronisation building block interface
- Ethernet switch management interface
- SPROM update interface

The current owner of each interface is either the IPMC or the host CPU.

Only the current owner has write access to the corresponding registers. The non-proprietor has only read access.

If the non-proprietor wants to become owner, it has to request ownership from the current owner. The current owner then has to grant ownership by inverting the bit corresponding to the interface.

Table 36: *Access Control Register*

Bit	Description	Default	Access
0	Indicates the current owner of the clock synchronisation building block interface 0: Host 1: IPMC	0_2	r/w
1	Indicates current owner of Ethernet switch management interface 0: Host 1: IPMC	1_2	r/w
2	Indicates the current owner of the SPROM update interface 0: Host 1: IPMC	0_2	r/w
7..3	Reserved	00000_2	r

A

Troubleshooting

Error List

A typical ATCA system is highly sophisticated. This chapter can be taken as an error list for detecting erroneous system configurations and strange behaviors. It cannot replace a serious and sophisticated presales and postsales support during application development.

If it is not possible to fix a problem with the help of this chapter, contact your local sales representative or Field Application Engineer (FAE) for further support.

Problem	Possible Reason	Solution
Blade does not work	Backplane voltage is too low.	Check that all backplane voltages are within their specific ranges. Check that power supply is capable to drive the respective loads.
Blade does not start	No valid BIOS was found.	Make sure a valid BIOS PROM is installed

B

Battery Exchange

Battery Exchange

The blade contains an on-board battery. Its location is shown in the following figure.

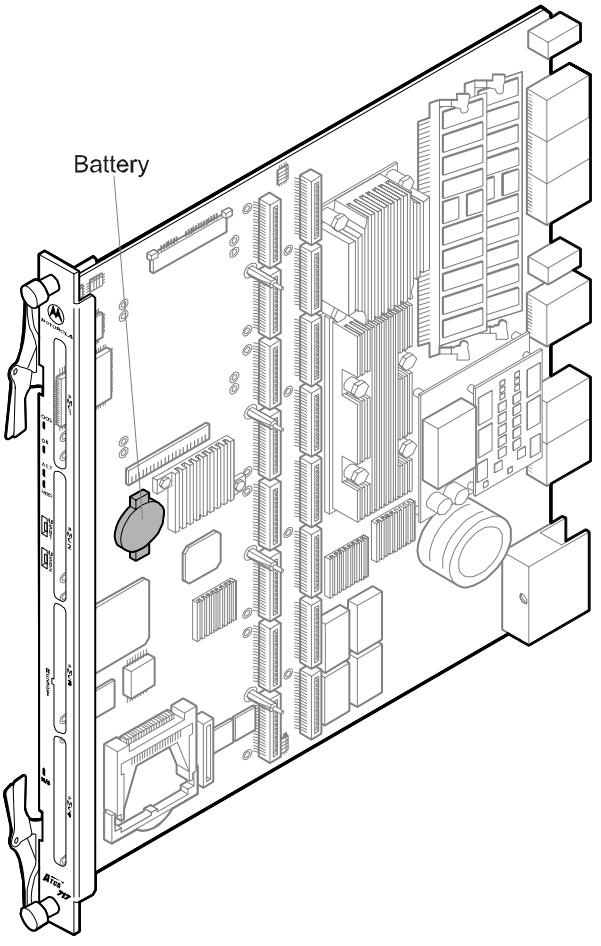

Figure 42: *Location of On-board Battery*

The battery provides data retention of seven years summing up all periods of actual data use. Motorola therefore assumes that there usually is no need to exchange the battery except, for example, in case of long-term spare part handling.

Caution

- **Board/System damage**
  Incorrect exchange of lithium batteries can result in a hazardous explosion. Therefore, exchange the battery as described in this chapter.

- **Data loss**
  If the battery does not provide enough power anymore, the RTC is initialized and the data in the NVRAM is lost.
  Therefore, exchange the battery before seven years of actual battery use have elapsed.

- **Data loss**
  Exchanging the battery always results in data loss of the devices which use the battery as power backup.
  Therefore, back up affected data before exchanging the battery.

- **Data loss**
  If installing another battery type than is mounted at board delivery may cause data loss since other battery types may be specified for other environments or may have a shorter lifetime.
  Therefore, only use the same type of lithium battery as is already installed.

Exchange Procedure

1. Remove old battery

PCB and battery holder damage
Removing the battery with a screw driver may damage the PCB or the battery holder.
To prevent this damage, do not use a screw driver to remove the battery from its holder.

2. Locate the ’+’ sign on the new battery. It indicates the positive terminal of the battery.
3. Insert the battery into the blade’s battery holder in such a way that the ’+’ on top of the battery is face up

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